PXI

NI PXI-4224/4225 User Manual

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Conventions

The following conventions are used in this manual:

<>	Angle brackets that contain numbers separated by an ellipsis represent a range of values associated with a bit or signal name—for example, PO.<3..0>.
»	The » symbol leads you through nested menu items and dialog box options to a final action. The sequence **File»Page Setup»Options** directs you to pull down the **File** menu, select the **Page Setup** item, and select **Options** from the last dialog box.
♦	The ♦ symbol indicates that the following text applies only to a specific product, a specific operating system, or a specific software version.
	This icon denotes a note, which alerts you to important information.
	This icon denotes a caution, which advises you of precautions to take to avoid injury, data loss, or a system crash. When this icon is marked on the product, refer to the *Read Me First: Safety and Radio-Frequency Interference* document, shipped with the product, for precautions to take.
	When symbol is marked on a product it denotes a warning advising you to take precautions to avoid electrical shock.
	When symbol is marked on a product it denotes a component that may be hot. Touching this component may result in bodily injury.
bold	Bold text denotes items that you must select or click in the software, such as menu items and dialog box options. Bold text also denotes parameter names.
italic	Italic text denotes variables, emphasis, a cross reference, hardware labels, or an introduction to a key concept. This font also denotes text that is a placeholder for a word or value that you must supply.
`monospace`	Text in this font denotes text or characters that you should enter from the keyboard, sections of code, programming examples, and syntax examples. This font is also used for the proper names of disk drives, paths, directories, programs, subprograms, subroutines, device names, functions, operations, variables, filenames and extensions, and code excerpts.
NI PXI-4224/4225	NI PXI-4224/4225 refers to both the NI PXI-4224 and the NI PXI-4225 module, unless otherwise noted.

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About the NI PXI-4224/4225

This chapter provides an introduction to the NI PXI-4224/4225 device and its installation.

The NI PXI-4224/4225 is part of the NI PXI-4200 series of data acquisition (DAQ) devices with integrated signal conditioning. The PXI-4200 series reduces measurement setup and configuration complexity by integrating signal conditioning and DAQ on the same product.

The NI PXI-4224/4225 is an 8-channel isolated analog input device with a ±10 V input range. It allows isolated analog measurements directly on the PXI platform, including isolated thermocouple measurements (NI PXI-4225 only). All eight channels are individually isolated.

The NI PXI-4225 has the following characteristics:

- Each channel has independent programmable gains and filters.
- An isolation rating of 150 V, Category II working voltage.
- The front connector is a 25-pin D-SUB connector, with 16 pins for analog input and 1 pin for reading CJC, +5 V, GND, and SPI communication. CJC, +5 V, GND, and SPI signals are not isolated.

The NI PXI-4224 has the following characteristics:

- Each channels has a gain of either 1 or 10.
- An isolation rating of 42 V, Category I.
- The front connector is a 25-pin D-SUB connector, with 16 pins for analog input and 1 pin for reading +5V, GND, and SPI communication. CJC, +5 V, GND, and SPI signals are not isolated.

Signal connections are made through a TB-2725 isothermal terminal block that provides connections for all eight analog input channels, as well as a CJC[1] sensor for making thermocouple measurements. You can optionally connect a standard 25-pin D-SUB cable to the device and cable it as needed for your application. If you construct a D-SUB connector you will lose the CJC capability of the NI PXI-4225.

Note Go to `ni.com/products` to determine if newly developed terminal blocks are available.

You can configure most settings on a per-channel basis through software. The NI PXI-4224/4225 is configured using Measurement & Automation Explorer (MAX) or through function calls to NI-DAQmx.

Note The NI PXI-4224/4225 is supported in NI-DAQmx only.

What You Need to Get Started

To set up and use the NI PXI-4224/4225, you need the following:

- ❑ Hardware
  - NI PXI-4224 or NI PXI-4225
  - One of the following:
    - TB-2725 terminal block
    - 25-pin D-SUB female connector
  - PXI or PXI/SCXI combination chassis
  - Sensors as required for your application
- ❑ Software
  - NI-DAQ 7.3.1 or later
  - One of the following:
    - LabVIEW
    - Measurement Studio
    - LabWindows™/CVI™

[1] The NI PXI-4224 does not have a CJC sensor.

- ❑ Documentation
  - – *NI PXI-4224/4225 User Manual*
  - – *Read Me First: Safety and Radio-Frequency Interference*
  - – *DAQ Quick Start Guide*
  - – PXI or PXI/SCXI combination chassis user manual
  - – Documentation for your software
- ❑ Tools
  - – 1/8 in. flathead screwdriver

You can download NI documents from `ni.com/manuals`.

National Instruments Documentation

The NI PXI-4224/4225 User Manual is one piece of the documentation set for your DAQ system. You could have any of several types of manuals depending on the hardware and software in your system. Use the manuals you have as follows:

- *DAQ Quick Start Guide*—This document describes how to install NI-DAQ devices and NI-DAQ. Install NI-DAQmx before you install the SCXI module.
- *SCXI Quick Start Guide*—This document describes how to set up an SCXI chassis, install SCXI modules and terminal blocks, and configure the SCXI system in MAX.
- PXI or PXI/SCXI combination chassis manual—Read this manual for maintenance information about the chassis and for installation instructions.
- Accessory installation guides or manuals—If you are using accessory products, read the terminal block installation guides. They explain how to physically connect the relevant pieces of the system.
- Software documentation—You may have both application software and NI-DAQmx software documentation. NI application software includes LabVIEW, Measurement Studio, and LabWindows/CVI. After you set up the hardware system, use either your application software documentation or the NI-DAQmx documentation to help you write your application. If you have a large, complicated system, it is worthwhile to look through the software documentation before you configure the hardware.

Installing the Application Software, NI-DAQ, and the DAQ Device

Refer to the *DAQ Quick Start Guide*, packaged with the NI-DAQ software, for instructions for installing your application software, NI-DAQ driver software, and the DAQ device to which you will connect the NI PXI-4224/4225.

NI-DAQ 7.3.1 or later is required to configure and program the NI PXI-4224/4225 device. If you do not have NI-DAQ 7.3.1 or later, you can either contact an NI sales representative to request it on a CD or download the it from `ni.com`.

Installing the NI PXI-4224/4225

Note Refer to the *Read Me First: Radio-Frequency Interference* document before removing equipment covers or connecting or disconnecting any signal wires.

Refer to the *DAQ Quick Start Guide* to unpack, install, and configure the NI PXI-4224/4225 in a PXI chassis and then to the *SCXI Quick Start Guide* if you are using a PXI/SCXI combination chassis.

LED Pattern Descriptions

The following LEDs on the NI PXI-4224/4225 front panel confirm the system is functioning properly:

- The *ACCESS* LED is normally green and blinks yellow for a minimum of 100 ms during the NI PXI-4224/4225 configuration.
- The *ACTIVE* LED is normally green and blinks yellow for a minimum of 100 ms during data acquisition.

2

Connecting Signals

This chapter provides details about the front signal connector of the NI PXI-4224/4225 and how to connect signals to the NI PXI-4224/4225.

Connecting Signals to the NI PXI-4224/4225

After you have verified that the NI PXI-4224/4225 is installed correctly and self-tested the device, refer to the following sections to connect signals to the device.

Caution Refer to the *Read Me First: Safety and Radio-Frequency Interference* document before removing equipment covers, or connecting or disconnecting any signal wires.

Front Signal Connector

The NI PXI-4224/4225 connection interface consists of a 25-pin D-SUB connector and one SMB connector. You can program SMB connector as a PFI 1 line or for external calibration. Tables 2-1 and 2-2 show the signal assignments of the D-SUB connector for the NI PXI-4225 and NI PXI-4224, respectively. Figures 2-1 and 2-2 show the front label, with each set of screw terminals labeled according to the corresponding differential input signal for the NI PXI-4225 and NI PXI-4224, respectively.

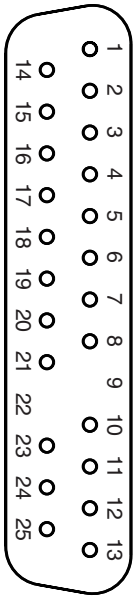
To connect a signal to the NI PXI-4225 or NI PXI-4224, use a TB-2725 terminal block designed specifically for the NI PXI-4225 and NI-PXI-4224, or use a 25-pin D-SUB to build a connector to suit your application. Refer to the *TB-2725 Isothermal Terminal Block Installation Guide* if you are using the TB-2725 terminal block. Use Tables 2-1and 2-2 to make the signal connections if you are constructing a connector using a 25-pin D-SUB connector.

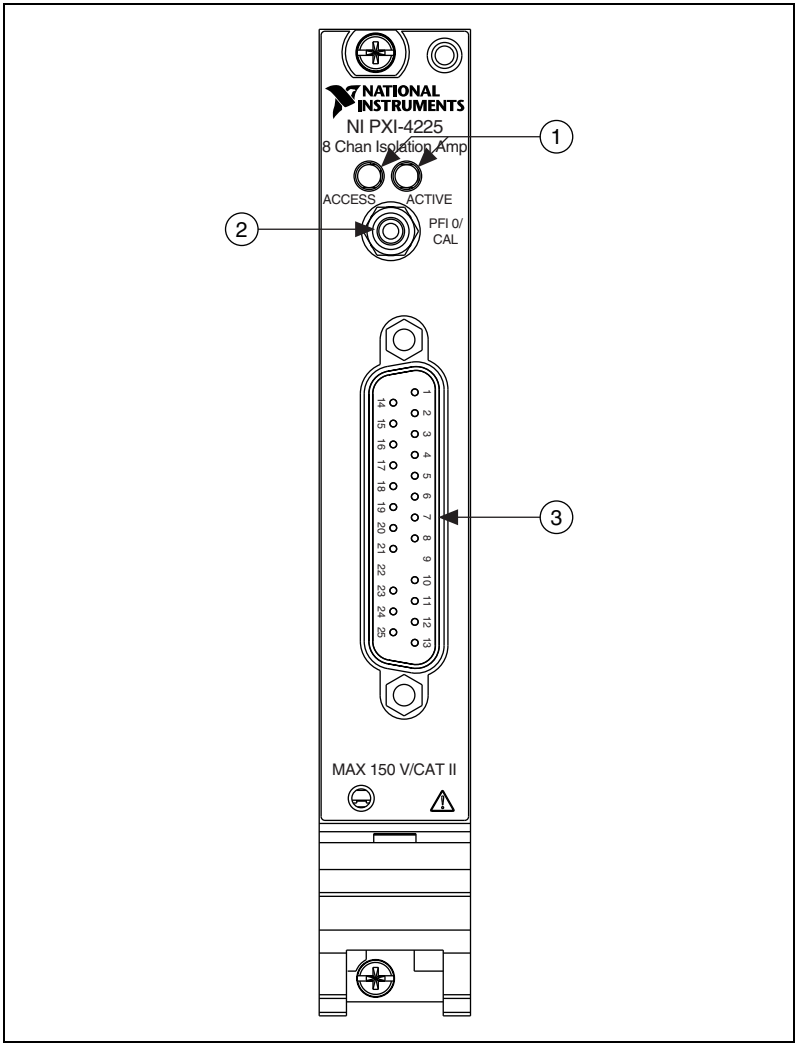
Connect a timing or triggering signal to the PFI 0/CAL SMB connector using a cable with an SMB signal connector.

Cautions The PFI 0/CAL SMB connector is for low-voltage timing and calibration signals *only.* Voltages greater than ±15 V can damage the device.

If you are building a 25-pin D-SUB connector for your application, make sure you use a connector and wires that are safety rated for the voltage and category of the signals in your application.

Table 2-1. NI PXI-4225 25-Pin D-SUB Terminal Pin Assignments

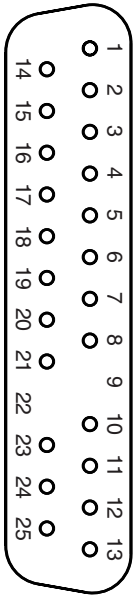
Front Connector Diagram	Pin Number	Signal Names	Pin Number	Signal Names
	14	AI 0 –	1	AI 0 +
	15	AI 1 –	2	AI 1 +
	16	AI 2 –	3	AI 2 +
	17	AI 3 –	4	AI 3 +
	18	AI 4 –	5	AI 4 +
	19	AI 5 –	6	AI 5 +
	20	AI 6 –	7	AI 6 +
	21	AI 7 –	8	AI 7 +
	22	No Pin	9	No Pin
	23	CJC +	10	D GND
	24	SPI CLK	11	MISO
	25	SELECT	12	MOSI
	N/A	N/A	13	+5 V

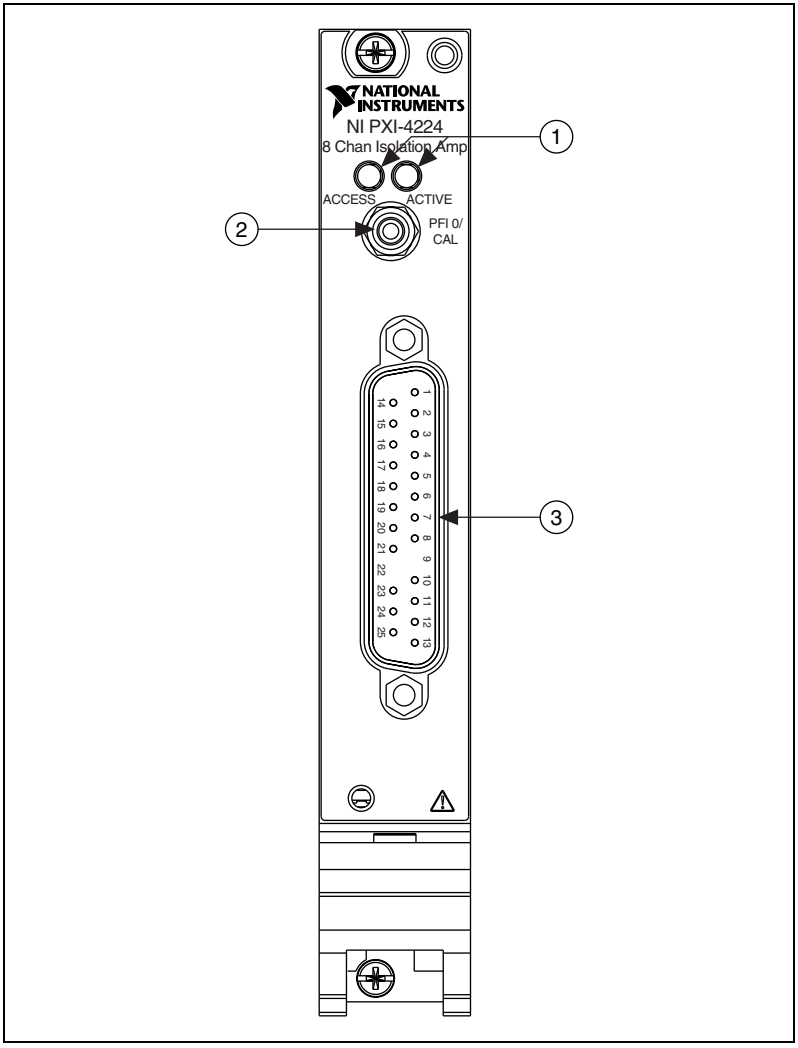


1	*ACCESS* and *ACTIVE* LEDs	3	25-Pin D-SUB or TB-2725 Terminal Block Connector
2	SMB PFI0/CAL Connector		

Figure 2-1. NI PXI-4225 Front Label

Table 2-2. NI PXI-4224 25-Pin D-SUB Terminal Pin Assignments

Front Connector Diagram	Pin Number	Signal Names	Pin Number	Signal Names
 NC–no connection	14	AI 0 –	1	AI 0 +
	15	AI 1 –	2	AI 1 +
	16	AI 2 –	3	AI 2 +
	17	AI 3 –	4	AI 3 +
	18	AI 4 –	5	AI 4 +
	19	AI 5 –	6	AI 5 +
	20	AI 6 –	7	AI 6 +
	21	AI 7 –	8	AI 7 +
	22	No Pin	9	No Pin
	23	NC	10	D GND
	24	SPI CLK	11	MISO
	25	SELECT	12	MOSI
	N/A	N/A	13	+5 V



1	*ACCESS* and *ACTIVE* LEDs	3	25-Pin D-SUB or TB-2725 Terminal Block Connector
2	SMB PFI0/CAL Connector		

Figure 2-2. NI PXI-4224 Front Label

Analog Input Connections

The following sections provide a definition of the signal source characteristics, descriptions of various ways to connect signals to the NI PXI-4224/4225, and electrical diagrams showing the signal source and connections. Whenever possible, use shielded twisted-pair field wiring and grounding, to reduce the effects of unwanted noise sources.

In the electrical diagrams, two different ground symbols are used. These symbols indicate that you cannot assume that the indicated grounds are at the same potential. Refer to Appendix A, *Specifications*, for maximum working voltage specifications.

You can make signal connections to the NI PXI-4224/4225 through either an NI terminal block, such as the TB-2725, or you can build a connector using a 25-pin D-SUB.

Caution If you are building a 25-pin D-SUB connector for your application, make sure you use a connector and signal wires that are safety rated for the voltage and category of the signals in your application.

Figures 2-3 through 2-6 illustrate connecting signals using a D-SUB connector.

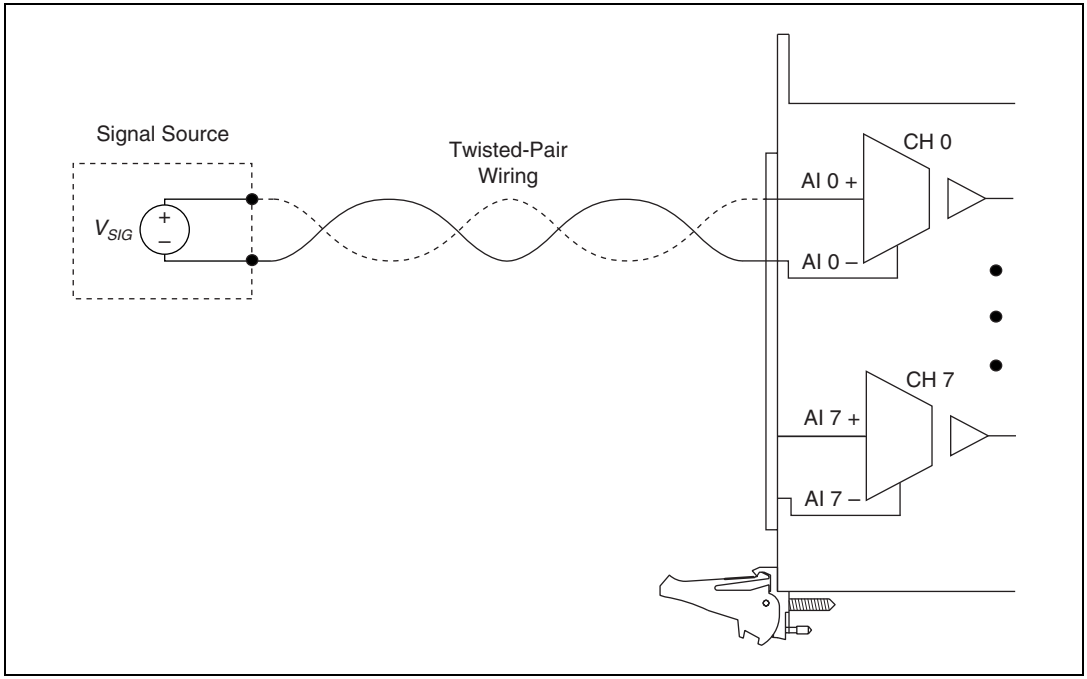


Figure 2-3. Unshielded Floating Signal Source Connection Using a D-SUB Connector

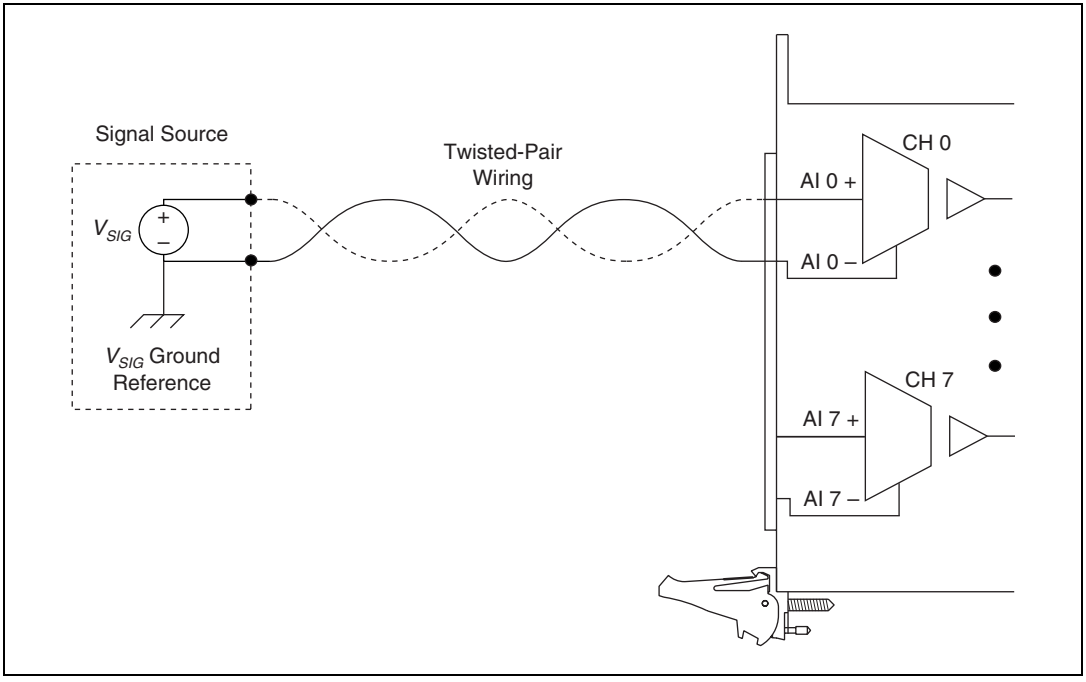


Figure 2-4. Unshielded Grounded Signal Source Connection Using a D-SUB Connector

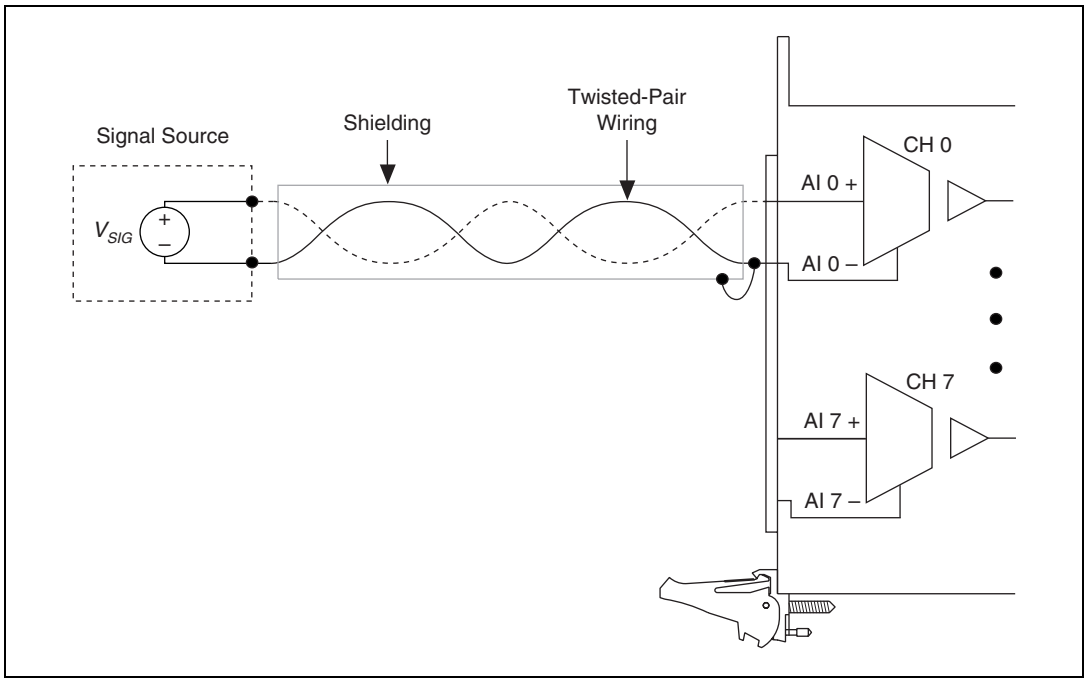


Figure 2-5. Shielded Floating Signal Source Connection Using a D-SUB Connector

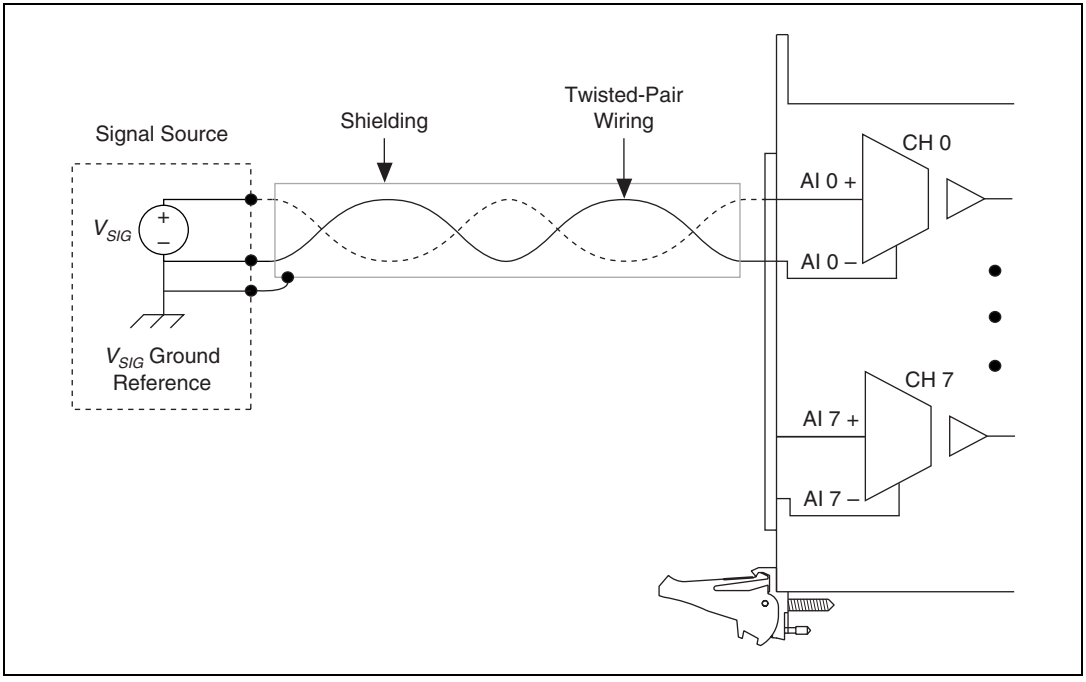


Figure 2-6. Shielded Grounded Signal Source Connection Using a D-SUB Connector

Figures 2-7 through 2-10 illustrate connecting signals using a terminal block.

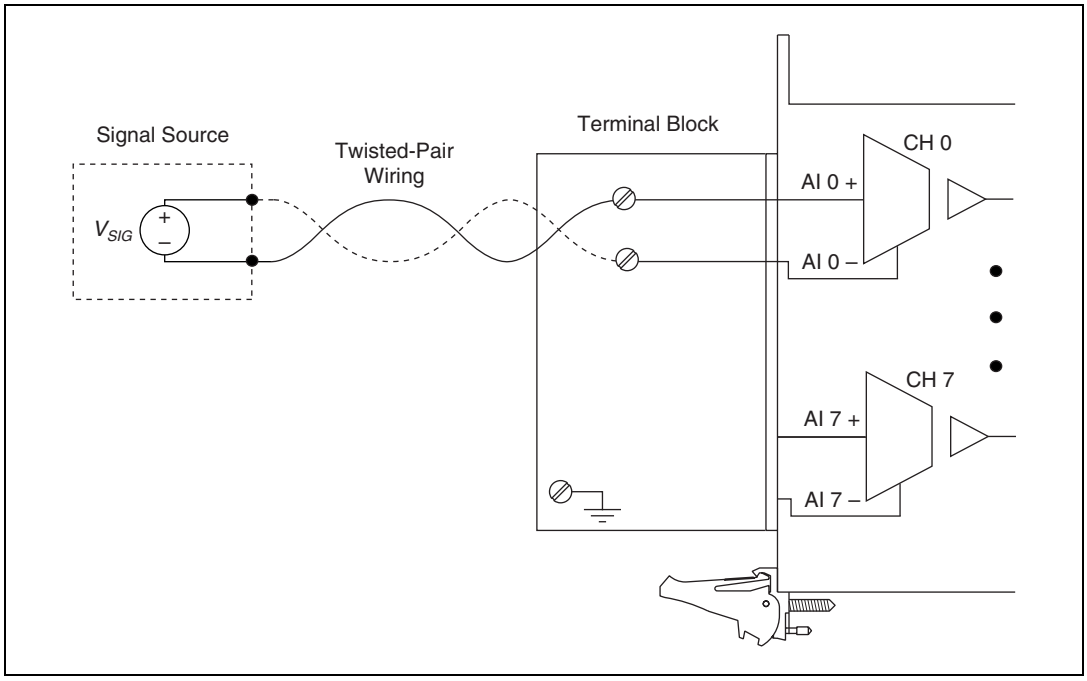


Figure 2-7. Unshielded Floating Signal Source Connection Using a Terminal Block

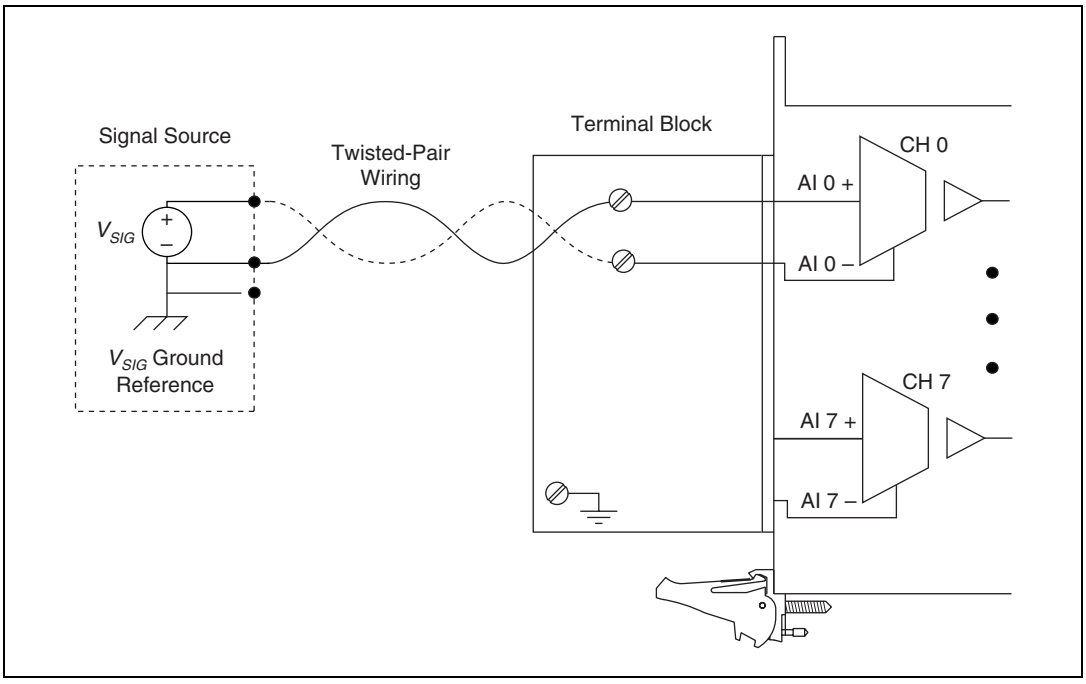


Figure 2-8. Unshielded Grounded Signal Source Connection Using a Terminal Block

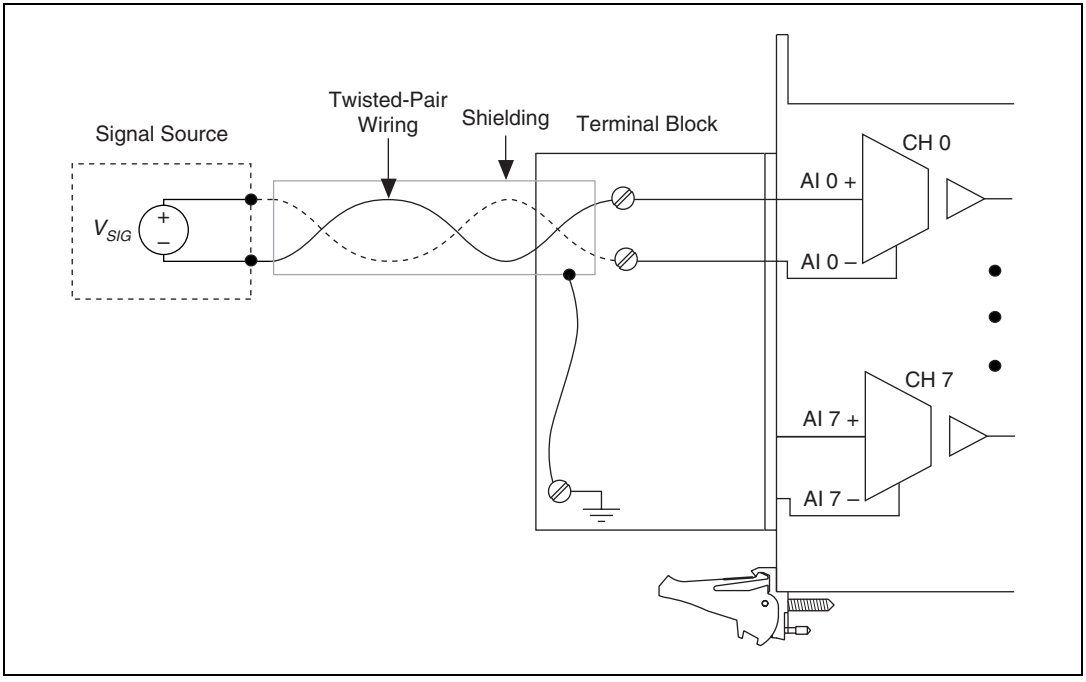


Figure 2-9. Shielded Floating Signal Source Connection Using a Terminal Block

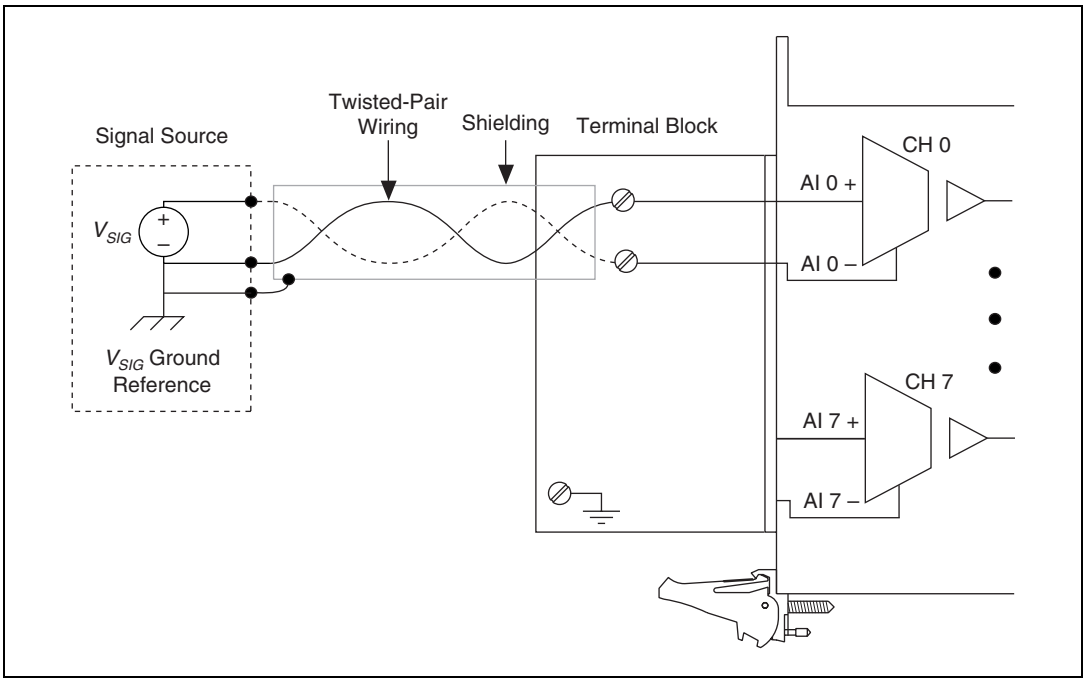


Figure 2-10. Shielded Grounded Signal Source Connection Using a Terminal Block

Floating Signal Source Connection

Figures 2-3, 2-5, 2-7, and 2-9 illustrate floating signal source connections. In this configuration, the signal source being measured is a floating signal source, such as a battery. A floating signal source is not connected in any way to the building ground system. In a floating signal source configuration, the measured input signal varies as the source floats outside the common-mode input range.

To connect a floating signal source connection to the NI PXI-4224/4225, the signal (V_{SIG}+) is connected to the NI PXI-4224/4225 channel (AI *X* +). The signal reference (V_{SIG}–) is connected to the channel reference (AI *X* –).

Ground-Referenced Signal Connection

Figures 2-4 2-6, 2-8, and 2-10 illustrate the ground-referenced signal connection. In this configuration, the voltage source being measured is referenced to its own ground reference that is connected through a conductive path to the instrument ground reference. For example, the path can be through a common earth ground or through the power line ground.

To connect a ground-reference signal source to the NI PXI-4224/4225, the signal (V_{SIG}+) is connected to the NI PXI-4224/4225 channel (AI *X* +). The signal reference (V_{SIG}–) is connected to the channel reference (AI *X* –).

Shielded Ground-Referenced Signal Connection (Recommended)

Figures 2-6 and 2-10 illustrate shielded ground-referenced signal connections. The connection to this signal source is identical to the ground-referenced signal connection with the addition of shielding around the field wiring. The shielding is grounded at the signal source ground (V_{SIG} Ground Reference). Connect the signal (V_{SIG}+) to the NI PXI-4224/4225 channel (AI *X* +). Connect the signal reference (V_{SIG}–) to the channel reference (AI *X* –).

This shielding scheme is effective at reducing capacitive or electrically coupled noise. The same concerns regarding the difference in ground potentials, discussed in the *Ground-Referenced Signal Connection* section, also apply to this configuration.

For more information about the function of the NI PXI-4224/4225 and other measurement considerations, refer to Chapter 4, *Theory of Operation*.

3

Configuring and Testing

This chapter provides details about configuring and testing the NI PXI-4224/4225 in MAX, including how to use device test panels and create and configure NI-DAQmx Tasks and NI-DAQmx Global Channels.

Verifying and Self-Testing the Signals Using Test Panels

After you have successfully installed the NI PXI-4224/4225, verified the installation, and connected the signals, use the NI PXI-4224/4225 device test panels to verify the device is measuring signals properly.

The test panels allow you to measure the signal connected to the NI PXI-4224/4225 directly as well as configure some of the properties of your measurement. To open the NI PXI-4224/4225 device test panels when in MAX, complete the following steps:

1. Expand **Devices and Interfaces** to display the list of devices and interfaces.
2. Expand **NI-DAQmx Devices** to display the list of NI-DAQmx devices.
3. Click **PXI-4225** or **PXI-4224**.
4. Click the **Test Panels** button in the device toolbar.
5. Configure the settings on the screen, and click **Start** to take a measurement.

To measure scaled voltages, further configure channel properties, and configure timing settings, use an **NI-DAQmx Task** or **NI-DAQmx Global Channel**.

Configuring the NI PXI-4224/4225 in MAX

This section describes how to create NI-DAQmx Tasks and NI-DAQmx Global Channels in MAX that allow you to take measurements with the NI PXI-4224/4225.

Creating a Voltage Task or Global Channel Using NI-DAQmx

An NI-DAQmx Global Channel gives a physical channel a name and provides scaling. An NI-DAQmx Task is a collection of channels with timing and triggering configured. To create a new NI-DAQmx Task or NI-DAQmx Global Channel, complete the following steps:

1. Double-click the **Measurement & Automation Explorer** icon on the desktop.
2. Right-click **Data Neighborhood** and select **Create New**.
3. Select **NI-DAQmx Task** or **NI-DAQmx Global Channel** and click **Next**.
4. Select **Analog Input** and select **Voltage**, and click **Next**.
5. If you are creating a task, keep the **Create New Local Channels** selected, and select the channels to add to the task. Select the channel(s) you want to configure for input voltage range. While making the selections you can select blocks of channels by pressing the <Shift> key or individual channels by pressing the <Ctrl> key. If you are creating a channel, you can select only one channel. Click **Next**.
6. Enter the name of the task or channel, and click **Finish**.
7. Select the channel(s) you want to configure for input voltage range. While making the selections you can select blocks of channels by pressing the <Shift> key or individual channels by pressing the <Ctrl> key.
8. Under the **Settings** tab, set the input range by entering the **Min** and **Max** values. You can also select the filter bandwidth settings for each channel.
9. Repeat steps 7 and 8 until you have configured all the channels.

Note For more information about how to further configure the NI PXI-4224/4225, or how to use LabVIEW to configure the device and take measurements, refer to Chapter 4, *Theory of Operation*.

Verifying and Self-Testing an NI-DAQmx Task or Global Channel

After you have created an analog input voltage NI-DAQmx Task or NI-DAQmx Global Channel, verify the NI-DAQmx Task or NI-DAQmx Global Channel signal and functionality using the **Test** button in the toolbar:

1. If you created an NI-DAQmx Task, set the timing and triggering settings you wish to use in the test in the **Task Timing** and **Task Triggering** tabs.
2. Click the **Test** button to open the test panel and take a measurement.

You have now verified the NI PXI-4224/4225 configuration and signal connection.

4

Theory of Operation

This chapter describes the theory of operation, measurement considerations, and timing information.

Theory of Operation

Figure 4-1 illustrates the key functional components of the NI PXI-4225, including the DAQ and integrated signal conditioning circuitry, and Figure 4-2 illustrates the NI PXI-4224.

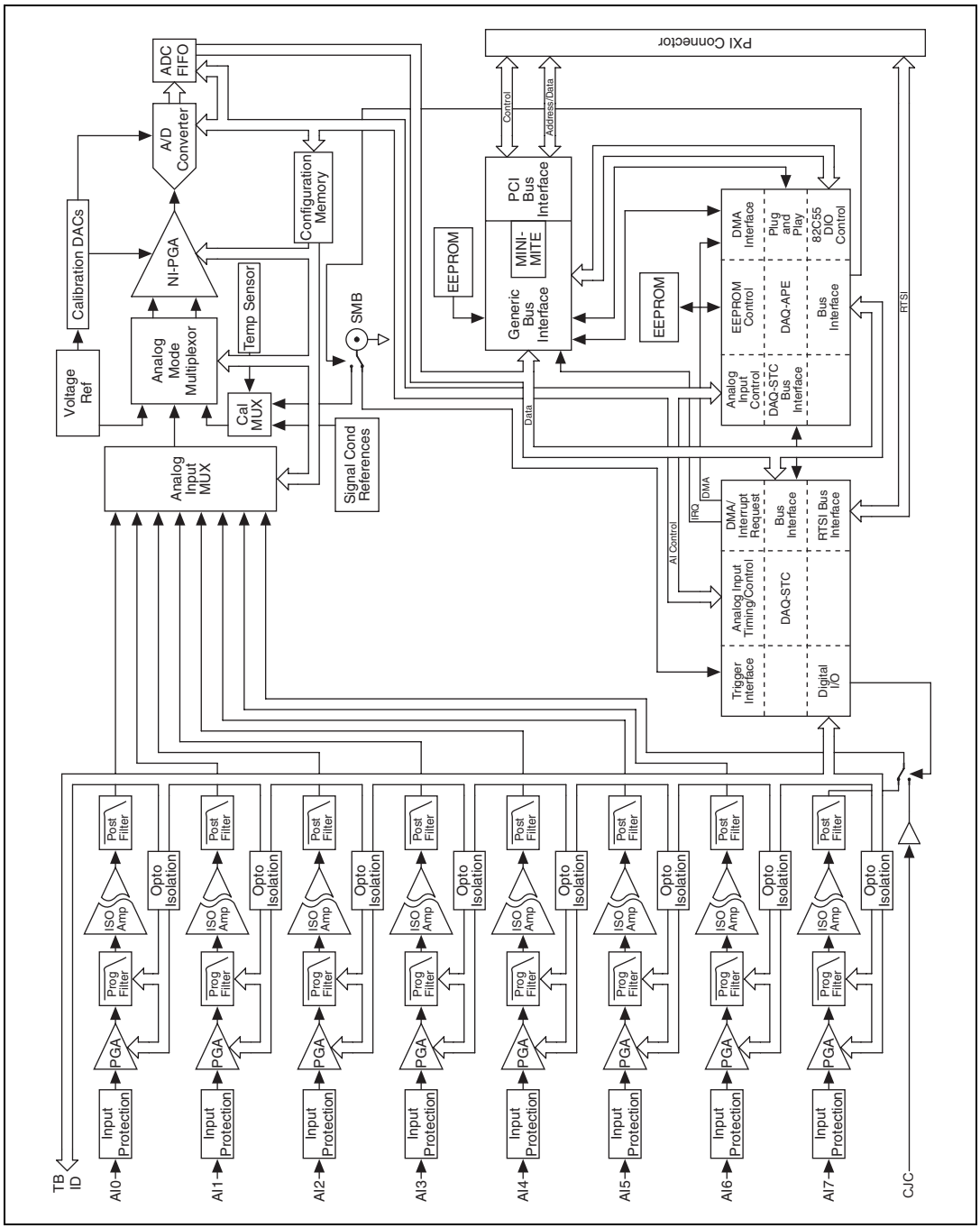


Figure 4-1. Block Diagram of NI PXI-4225

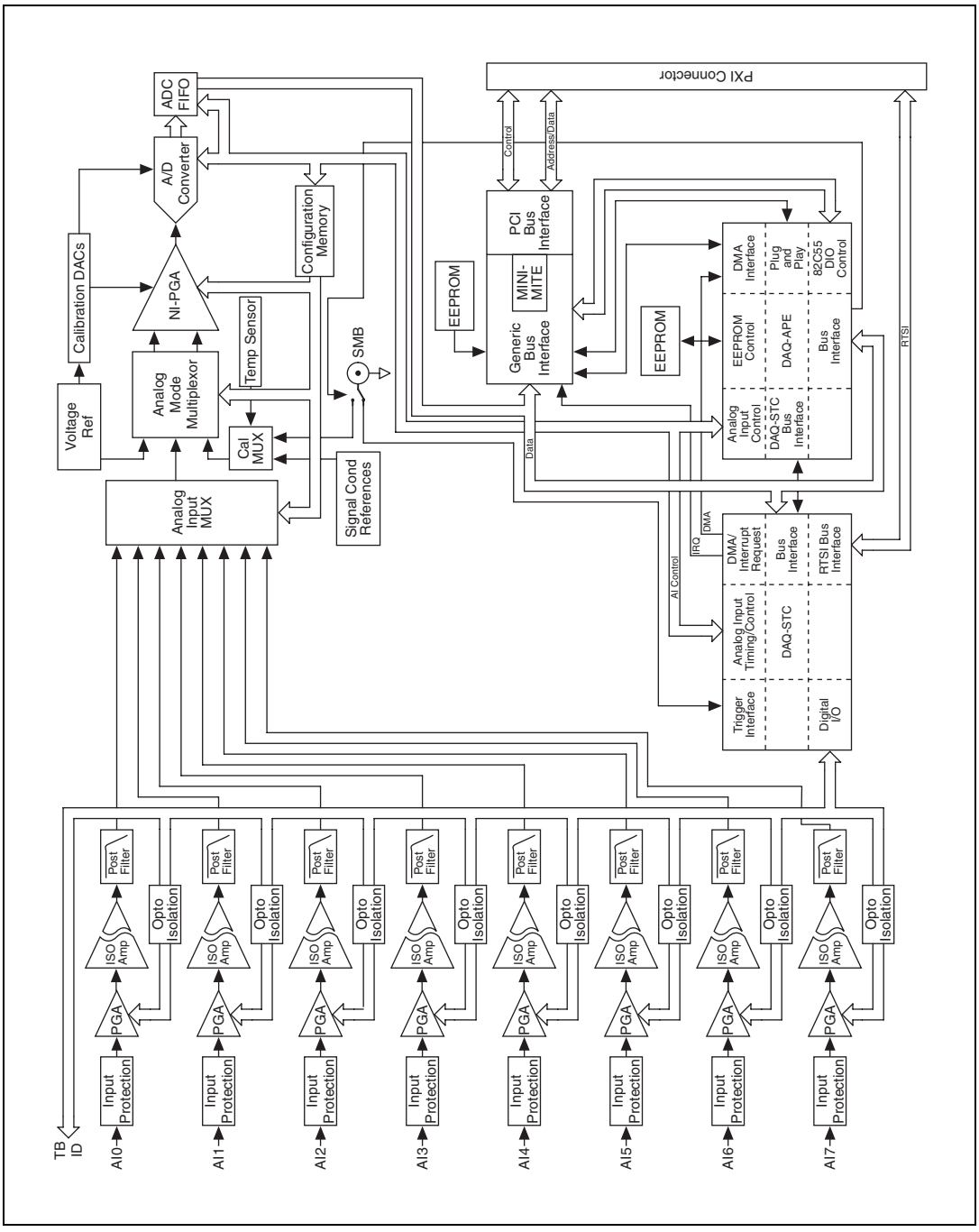


Figure 4-2. Block Diagram of NI PXI-4224

Signal Conditioning Functional Overview

The NI PXI-4224/4225 is part of the PXI-4200 series of DAQ devices with integrated signal conditioning designed to provide application-specific signal conditioning, DAQ, and integrated field wiring connectivity on the same product. The NI PXI-4224/4225 signal conditioning circuitry is designed to provide attenuation, amplification, and filtering capabilities as described in Table 4-1.

Table 4-1. Signal Conditioning Functional Blocks

Signal Conditioning Component	Description
Input Protection	Each NI PXI-4224/4225 channel has overvoltage protection in the event that a channel is improperly wired.
PGA	Each channel has a programmable gain amplifier. The available gains on the NI PXI-4225 are 1, 2, 5, 10, 20, 50, 100, 200, 500, and 1000, which covers the input range of ±10 mV to ±10 V. The available gains on the NI PXI-4224 are 1 and 10, which covers the input range of ±1 V to ±10 V. All of the gains cover the input ranges of ±10 V to ±10 mV. The DAQ gain is always set to ±10.
Programmable Filter (NI PXI-4225 only)	Each channel has a 3-Pole Butterworth filter. You can program the filter with a bandwidth of 10 Hz, 10 kHz, or bypassed.
Isolation Amplifier	Each channel has an isolation amplifier that creates true channel-to-channel isolation.
Post Filter	A post filter is provided to clean up noise spikes created by the isolation amplifier.

Measurement Considerations

This section provides more information about the type of signal connection made to the NI PXI-4224/4225 and important factors that can affect your measurement.

Input Impedance

Figure 4-3 illustrates the input impedance of an NI PXI-4224/4225 and its effect on the measurement of a circuit under test. If you know the source impedance of the circuit under test, you can correct for the attenuation caused by the NI PXI-4224/4225 in software. Since R_{IN} is relatively large (1 GΩ), it requires a large source impedance, R_S, to cause a significant

change in the measured voltage, V_{MEAS}. In general, a source impedance of less than 200 kΩ does not interfere with the accuracy of the measurement. For example, a 200 kΩ source impedance results in a 0.02% gain error.

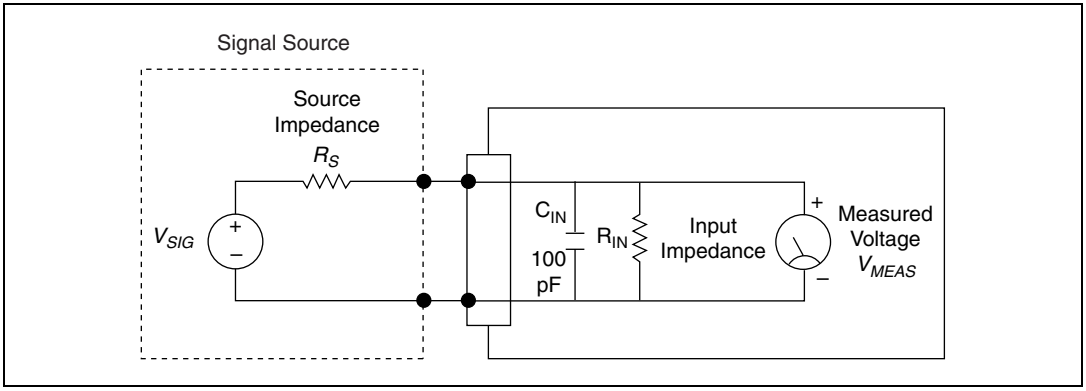


Figure 4-3. Effect of Input Impedance on Signal Measurements

Although R_S does not influence DC measurements, take care when measuring AC signals since C_{IN} attenuates higher frequencies if R_S is too large. For example:

$$V_{MEAS} = \frac{V_{SIG}R_{IN}}{R_S + R_{IN}}$$

$$Bandwidth = \frac{1}{2\pi R_S C_{IN}}$$

Common-Mode Rejection Ratio

The ability of a measurement device to reject voltages that are common to both input terminals is referred to as the common-mode rejection ratio (CMRR). The CMMR is usually stated in decibels at a given frequency or over a given frequency band of interest. Common-mode signals can arise from a variety of sources and can be induced through conductive or radiated means. One of the most common sources of common-mode interference is 50 or 60 Hz powerline noise.

The minimum NI PXI-4224/4225 CMRR is 140 dB, which results in a reduction of CMV by a factor of 10,000,000.

Normal-Mode Rejection

- NI PXI-4225

Normal-mode rejection (NMR) refers to the ability of the NI PXI-4225 to reject a differentially (normally) applied signal when the NI PXI-4225 filters are set to 10 Hz. The NMR is a function of the lowpass filter characteristics and is quantified in the normal-mode rejection ratio (NMRR) specification, which specifies the capability of the NI PXI-4225 to reject a differentially applied unwanted 60 Hz signal. In the case of the NI PXI-4225, this specification is 43 db at 50 Hz and 47 db at 60 Hz with a 10 Hz filter setting. This NMR is usually only applicable when taking DC measurements. The NMRR is specified at the powerline frequencies because most measurement noise arises there.

Effective CMR

When the frequency of a common-mode signal is known and outside of the measurement frequency band of interest, you can use an analog or digital filter, or both, to further reduce the residual error left from the finite CMRR of the instrument. The combined CMR of the instrument and the filter attenuation results in an effective CMR. When expressed in decibels, the effective CMR is equal to the sum of the CMRR and the attenuation due to the filter at a specified frequency.

Timing and Control Functional Overview

The NI PXI-4224/4225 is based on the NI E Series DAQ device architecture. This architecture uses the NI data acquisition system timing controller (DAQ-STC) for time-related functions. The DAQ-STC consists of two timing groups that control AI and general-purpose counter/timer functions. These groups include a total of seven 24-bit and three 16-bit counters and a maximum timing resolution of 50 ns. The DAQ-STC makes possible applications such as equivalent time sampling, and seamless changing of the sampling rate.

The NI PXI-4224/4225 uses the PXI trigger bus to easily synchronize several measurement functions to a common trigger or timing event. The PXI trigger bus is connected through the rear signal connector to the PXI chassis backplane. The DAQ-STC provides a flexible interface for connecting timing signals to other devices or external circuitry. The NI PXI-4224/4225 uses the PXI trigger bus to interconnect timing signals between PXI devices, and the programmable function input (PFI) pin on the front SMB connector to connect the device to external circuitry. These

connections are designed to enable the device to both control and be controlled by other devices and circuits.

The DAQ-STC has internal timing signals you can control by an external source. These timing signals also can be controlled by signals internally generated to the DAQ-STC, and these signals are software configurable. Figure 4-4 shows an example of the signal routing multiplexer controlling the AI CONVERT CLOCK signal.

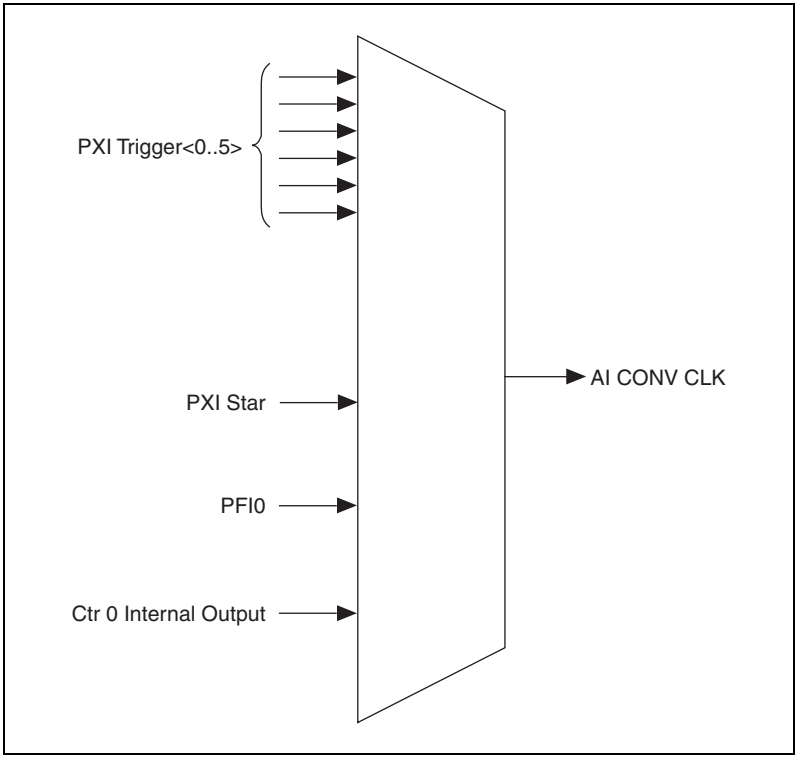


Figure 4-4. AI CONV CLK Signal Routing

Figure 4-4 shows that AI CONV CLK can be generated from a number of sources, such as the external signals PFI0, PXI_Trig<0..5>, and PXI_Star, and the Ctr 0 Internal Output.

Programmable Function Inputs

PFI0 is connected to the front SMB connector of the NI PXI-4224/4225. Software can select PFI0 as the external source for a given timing signal. Any timing signal can use the PFI0 pin as an input, and multiple timing signals can simultaneously use the same PFI. This flexible routing scheme reduces the need to change physical connections to the I/O connector for different applications. Refer to Table 4-2 for information regarding the available PFI0 signals.

Device and PXI Clocks

Many functions performed by the NI PXI-4224/4225 require a frequency timebase to generate the necessary timing signals for controlling A/D conversions, digital-to-analog converter (DAC) updates, or general-purpose signals at the I/O connector.

The NI PXI-4224/4225 can use either its internal 20 MHz master timebase or a timebase received over the PXI trigger bus on the PXI clock line. These timebases are software configurable. If you configure the device to use the internal timebase, you can program the device to drive its internal timebase over the PXI trigger bus to another device programmed to receive this timebase signal. This clock source, whether local or from the PXI trigger bus, is used directly by the device as the primary frequency source. The default configuration is to use the internal timebase without driving the PXI trigger bus timebase signal. The NI PXI-4224/4225 can use the PXI_Trig<7> line to synchronize `Master Timebase` with other devices.

For the NI PXI-4224/4225, PXI Trig<0..5>, and PXI_Star, connect through the NI PXI-4224/4225 backplane. The PXI Star Trigger line allows the NI PXI-4224/4225 to receive triggers from any Star Trigger controller plugged into slot 2 of the chassis. For more information about the Star Trigger, refer to the *PXI Hardware Specification, Revision 2.1* and *PXI Software Specification, Revision 2.1*.

Figure 4-5 shows this signal connection scheme.

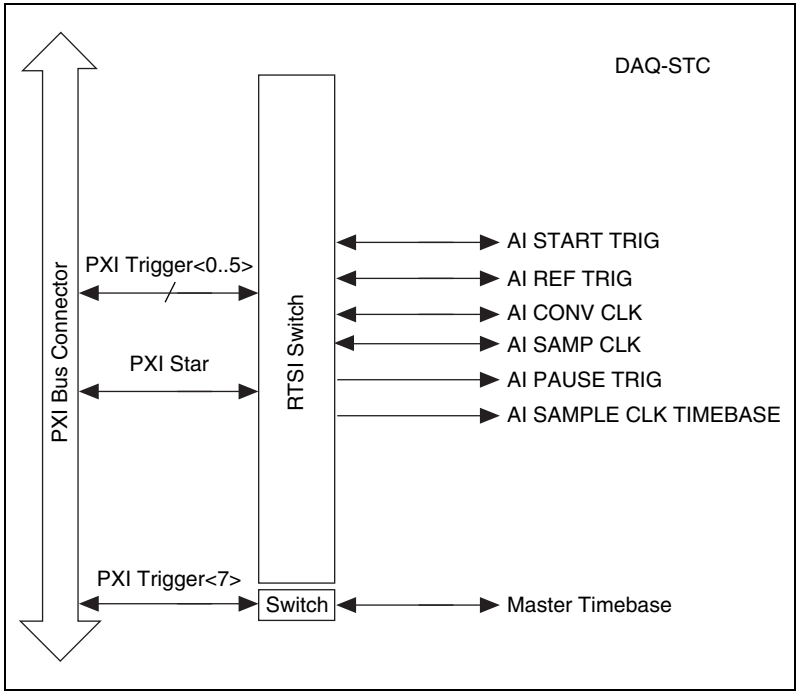


Figure 4-5. NI PXI-4224/4225 PXI Trigger Bus Signal Connection

Table 4-2 provides more information about each of the timing signals available on the PXI trigger bus. For more detailed timing signal information, refer to Appendix B, *Timing Signal Information*.

Table 4-2. PXI Trigger Bus Timing Signals

Signal	Direction	Description	Availability on PFI0 SMB	Availability on PXI Trigger Bus
AI START TRIG	Input	This trigger is the source for the analog input digital start trigger, which is the trigger that begins an acquisition.	Input	Input
	Output	This trigger sends out the actual analog input start trigger.	Output	Output
AI PAUSE TRIG	Input	This signal can pause and resume acquisition.	Input	Input
AI SAMPLE CLK TIMEBASE	Input	This timebase provides the master clock from which the sample clocks are derived.	Input	Input
AI HOLD COMPLETE	Output	This signal is output when the analog signal to be converted by the ADC has been held.	Not available	Not available

5

Using the NI PXI-4224/4225

This chapter describes how to program the NI PXI-4224/4225, using DAQ Assistant or LabVIEW, and how to calibrate the device.

Developing Your Application

This section describes the software and programming steps necessary to use the NI PXI-4224/4225. For more information about a particular software or programming process, refer to your ADE documentation.

Typical Program Flow Chart

Figure 5-1 shows a typical program flow chart for creating an AI voltage channel, taking a measurement, and clearing the data.

Note For more information about creating tasks and channels in MAX, refer to Chapter 3, *Configuring and Testing*.

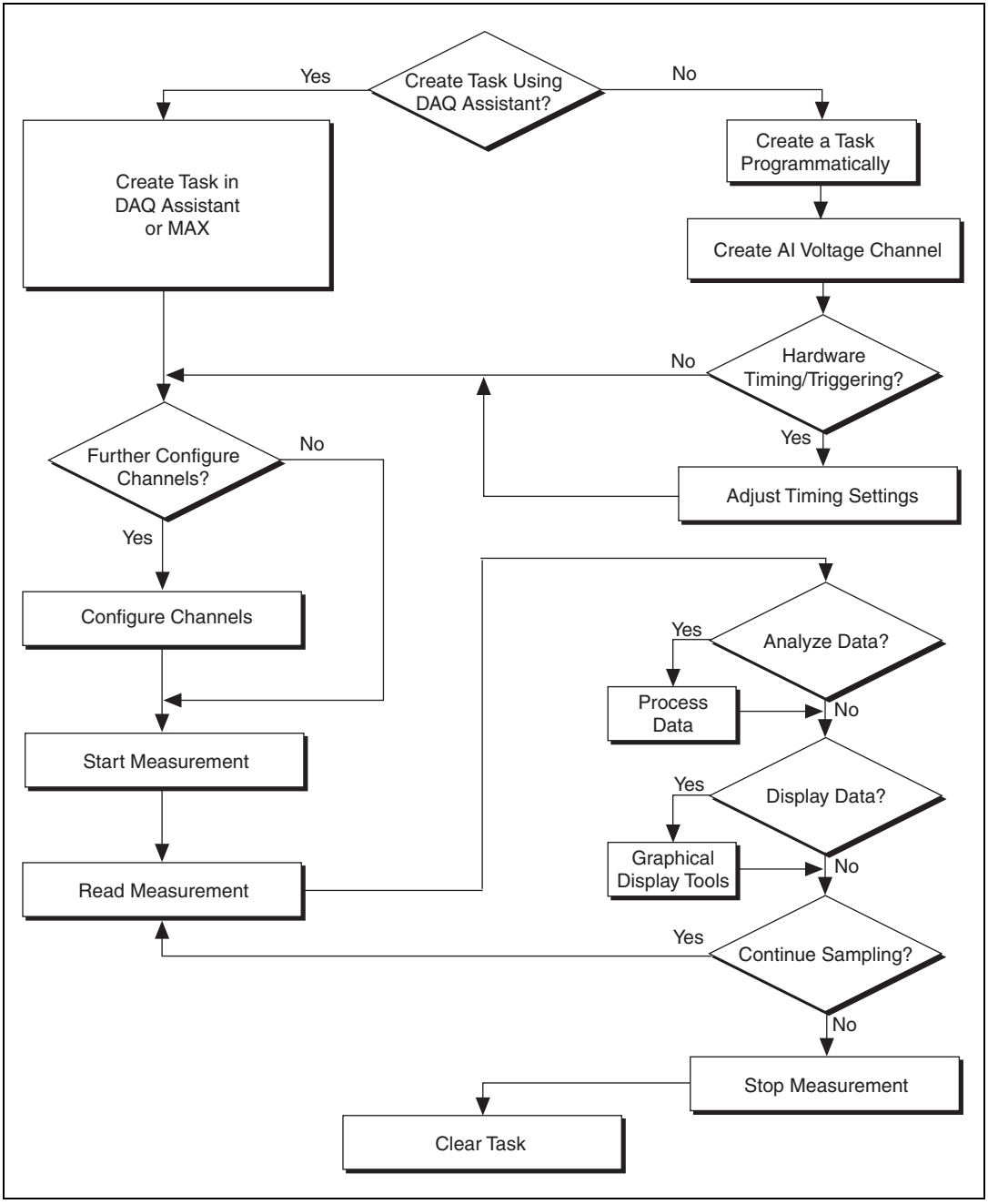


Figure 5-1. Typical Program Flowchart

Overview of Typical Flow Chart

The following sections briefly discuss some considerations for some of the steps in Figure 5-3. These sections are meant to provide an overview of some of the options and features available when programming with NI-DAQmx.

Creating a Task Using DAQ Assistant or Programmatically

When creating an application, you must first decide whether to create the task using the DAQ Assistant or programmatically in the ADE.

Developing your application using NI-DAQmx allows you to configure most settings such as measurement type, selection of channels, input limits, task timing, and task triggering using the DAQ Assistant tool. You can access the DAQ Assistant either through MAX or through your NI ADE. Choosing to use the DAQ Assistant can simplify the development of your application. When using a sensor that requires complex scaling, or when many properties differ between channels in the same task, NI recommends creating tasks using the DAQ Assistant for ease of use.

If you are using an ADE other than an NI ADE, or if you want to explicitly create and configure a task for a certain type of acquisition, you can programmatically create the task from your ADE using function or VI calls. If you create a task using the DAQ Assistant, you can still further configure the individual properties of the task programmatically using function calls or property nodes in your ADE. NI recommends creating a task programmatically if you need explicit control of programmatically adjustable properties of the DAQ system. Programmatically creating tasks is also recommended if you are synchronizing multiple devices using master and slave tasks. Refer to the *Synchronizing the NI PXI-4224/4225* section for more information about synchronizing multiple NI PXI-4225 devices.

Programmatically adjusting properties for a task created in the DAQ Assistant overrides the original settings only for that session. The changes are *not* saved to the task configuration. The next time you load the task, the task uses the settings originally configured in the DAQ Assistant.

Adjusting Timing and Triggering

There are several timing properties that you can configure either through the DAQ Assistant or programmatically using function calls or property nodes in your application. If you create a task in the DAQ Assistant, you still can modify the timing properties of the task programmatically in your application.

When programmatically adjusting timing settings, you can set the task to acquire continuously, acquire a buffer of samples, or acquire one point at a time. For continuous and buffered acquisitions, you can set the acquisition rate and the number of samples to read. By default, the clock settings are automatically set by an internal clock based on the requested sample rate. You also can select advanced features such as clock settings that specify an external clock source, the internal routing of the clock source, or that select the active edge of the clock signal. You can also specify whether or not to start the acquisition using a start trigger signal.

Configuring Channel Properties

All of the different ADEs used to configure the NI PXI-4224/4225 access an underlying set of NI-DAQmx properties. Table 5-1 lists of some of the properties that configure the NI PXI-4224/4225. You can use this list to determine which of properties you need to set to configure the device for your application. If you created the task and channels using the DAQ Assistant, you can still modify the channel properties programmatically. For a complete list of NI-DAQmx properties, refer to your ADE help file.

Table 5-1. NI-DAQmx Properties

Property	Short Name	Description
Analog Input» General Properties» Input Configuration» Coupling Property	`AI.Coupling`	DC—Allows NI-DAQmx to measure the input signal. GND—Removes the signal source from the measurement and measures only ground.
Analog Input»General Properties»Filter» Analog Lowpass»Enable (NI PXI-4225 only)	`AI.Lowpass.Enable`	Enables the lowpass filter of the channel.

Table 5-1. NI-DAQmx Properties (Continued)

Property	Short Name	Description
Analog Input»General Properties»Filter»Analog Lowpass»Cutoff Frequency (NI PXI-4225 only)	`AI.Lowpass.CutoffFreq`	Specifies in hertz the frequency corresponding to the –3dB cutoff of the filter. You can specify either 10.0 or 10000.0.
Analog Input»General Properties»Gain	`AI.Gain`	Specifies the gain of the isolation amplifier. For the NI PXI-4225 you can specify 1, 2, 5, 10, 20, 50, 100, 200, 500, or 1000. For the NI PXI-4224 you can specify 1 or 10.
Analog Input»General Properties»Advanced» High Accuracy Settings» Auto Zero Mode	`AI.AutoZeroMode`	Specifies when to measure ground. NI-DAQmx subtracts the measured ground voltage from every sample.

Note Table 5-1 is a representative sample of important properties you can adjust in analog input measurements with the NI PXI-4224/4225. It is *not* a complete list of NI-DAQmx properties and does not include every property you may need to configure the device. For a complete list of NI-DAQmx properties and more information about NI-DAQmx properties, refer to your ADE help file.

Acquiring, Analyzing, and Presenting

After configuring the task and channels, you can start your acquisition, read measurements, analyze the data returned, and display it according to the needs of your application. Typical methods of analysis include digital filtering, averaging data, performing harmonic analysis, applying a custom scale, or adjusting measurements mathematically.

NI provides powerful analysis toolsets for each NI ADE to assist non-programmers in performing advanced data analysis. After you acquire the data and perform any required analysis, it is useful to display the data in a graphical form or log it to a file. NI ADEs provide easy-to-use tools for graphical display, such as charts, graphs, slide rules, and gauge indicators. NI ADEs have tools that allow you to save the data to files such as spreadsheets for easy viewing, ASCII files for universality, or binary files for smaller file sizes.

Completing the Application

After you have completed the measurement, analysis, and presentation of the data, it is important to stop and clear the task. This releases any memory used by the task and frees up the DAQ hardware for use in another task.

Developing an Application Using LabVIEW

This section describes in more detail the steps shown in Figure 5-1, *Typical Program Flowchart*, such as how to create a task in LabVIEW and configure the channels of the NI PXI-4224/4225. For further instructions, select **Help»VI, Function, & How-To Help** from the LabVIEW menu bar.

Note Except where otherwise stated, the VIs in Table 5-2 are located on the **Functions» All Functions»NI Measurements»DAQmx - Data Acquisition** subpalette and accompanying subpalettes in LabVIEW.

Table 5-2. Programming a Task in LabVIEW

Flowchart Step	VI or Program Step
Create Task in DAQ Assistant	Create a `DAQmx Task Name Constant` located on the **Controls»All Controls»I/O»DAQmx Name Controls** subpalette, right-click it, and select `New Task (DAQ Assistant)`.
Create a Task Programmatically (optional)	`DAQmx Create Task.vi`—This VI is optional if you created and configured your task using the DAQ Assistant. However, if you use it in LabVIEW any changes you make to the task will not be saved to a task in MAX.
Create AI Voltage Channel (optional)	`DAQmx Create Virtual Channel.vi` (AI Voltage by default)—This VI is optional if you created and configured your task and channels using the DAQ Assistant.
Adjust Timing Settings (optional)	`DAQmx Timing.vi` (Sample Clock by default)—This VI is optional if you created and configured your task using the DAQ Assistant.
Configure Channels (optional)	DAQmx Channel Property Node—Refer to the *Using a DAQmx Channel Property Node in LabVIEW* section for more information. This step is optional if you created and fully configured the channels in your task using the DAQ Assistant.
Start Measurement	`DAQmx Start Task.vi`

Table 5-2. Programming a Task in LabVIEW (Continued)

Flowchart Step	VI or Program Step
Read Measurement	`DAQmx Read.vi`
Analyze Data	Some examples of data analysis include filtering, scaling, harmonic analysis, or level checking. Some data analysis tools are located on the **Functions»Signal Analysis** subpalette and on the **Functions»All Functions»Analyze** subpalette.
Display Data	You can use graphical tools such as charts, gauges, and graphs to display your data. Some display tools are located on the **Controls»Numeric Indicators** subpalette and **Controls» All Controls»Graph** subpalette.
Continue Sampling	For continuous sampling, use a While Loop. If you are using hardware timing, you also need to set the `DAQmx Timing.vi` sample mode to Continuous Samples. To set the VI, right-click the terminal of the `DAQmx Timing.vi` labeled **sample mode** and click **Create»Constant**. Click the box and select **Continuous Samples**.
Stop Measurement	`DAQmx Stop Task.vi`—This VI is optional. Clearing the task will automatically stop the task.
Clear Task	`DAQmx Clear Task.vi`

Using a DAQmx Channel Property Node in LabVIEW

Note With the NI PXI-4225, you must use property nodes to change filter settings.

You can use property nodes in LabVIEW to manually configure your channels. To create a LabVIEW property node, complete the following steps:

1. Launch LabVIEW.
2. You can create the property node in a new VI or in an existing VI.
3. Open the block diagram view.
4. From the **All Functions** toolbox, select **All Functions» NI Measurements»DAQmx - Data Acquisition**, and select `DAQmx Channel Property Node`.

5. Left-click inside the **Property** box and select **Active Channels**. This allows you to specify exactly what channel(s) you want to configure. If you want to configure several channels with different properties, separate the lists of properties with another **Active Channels** box, and assign the appropriate channel to each list of properties.

Note If you do not use Active Channels, the properties will be set on all of the channels in the task.

6. Right-click **ActiveChan** and select **Add Element**. Left-click the new **ActiveChan** box and go to **Properties**. Navigate through the menus and select the property you wish to define.
7. You must change the property to read or write to either get the property or write a new value. Right-click the property, go to **Change To**, and select **Write**, **Read**, or **Default Value**.
8. Once you have added the property to the property node, right-click the terminal to change the attributes of the property, or to add a control, constant, or indicator.
9. To add another property to the property node, right-click an existing property and left-click **Add Element**. To change the new property, left-click it and select the property you wish to define. You can also drag the bottom of the property node down to add more channels to the node.

Note Refer to the *LabVIEW Help* for information about property nodes and specific NI-DAQmx properties.

Synchronization and Triggering

If you have multiple NI PXI-4224/4225 devices, you can synchronize them to acquire samples at the same time and at the same rate. You can use multiple NI PXI-4224/4225 devices to acquire and analyze complex signals.

For multiple NI PXI-4224/4225 devices to start an acquisition simultaneously, they all must reference a common start trigger. To prevent drift over the course of the acquisition, they must share a common timebase or sample clock.

The NI PXI-4224/4225 that generates the start trigger and the timebase for all of the synchronized devices is called the *master*. The master NI PXI-4224/4225 exports the shared timing signals through the PXI bus to the slave devices.

Each NI PXI-4224/4225 contains a DAQ-STC chip that is capable of generating a hardware sample clock based on its timebase clock and start trigger. When using a shared timebase and start trigger, each slave NI PXI-4225 still generates a hardware sample clock, but it generates the clock using the timebase and start trigger of the master NI PXI-4224/4225. This causes the slave device to acquire samples at the same time as the master.

The preferred method of synchronization is to use a shared timebase, but it is also possible to synchronize multiple NI PXI-4224/4225 devices by sharing the sample clock between them. This manual only discusses the shared timebase method.

Synchronizing the NI PXI-4224/4225

Figure 5-2 shows a typical program flowchart for synchronizing the sample clocks and start triggers of two devices, taking a measurement, and clearing the data.

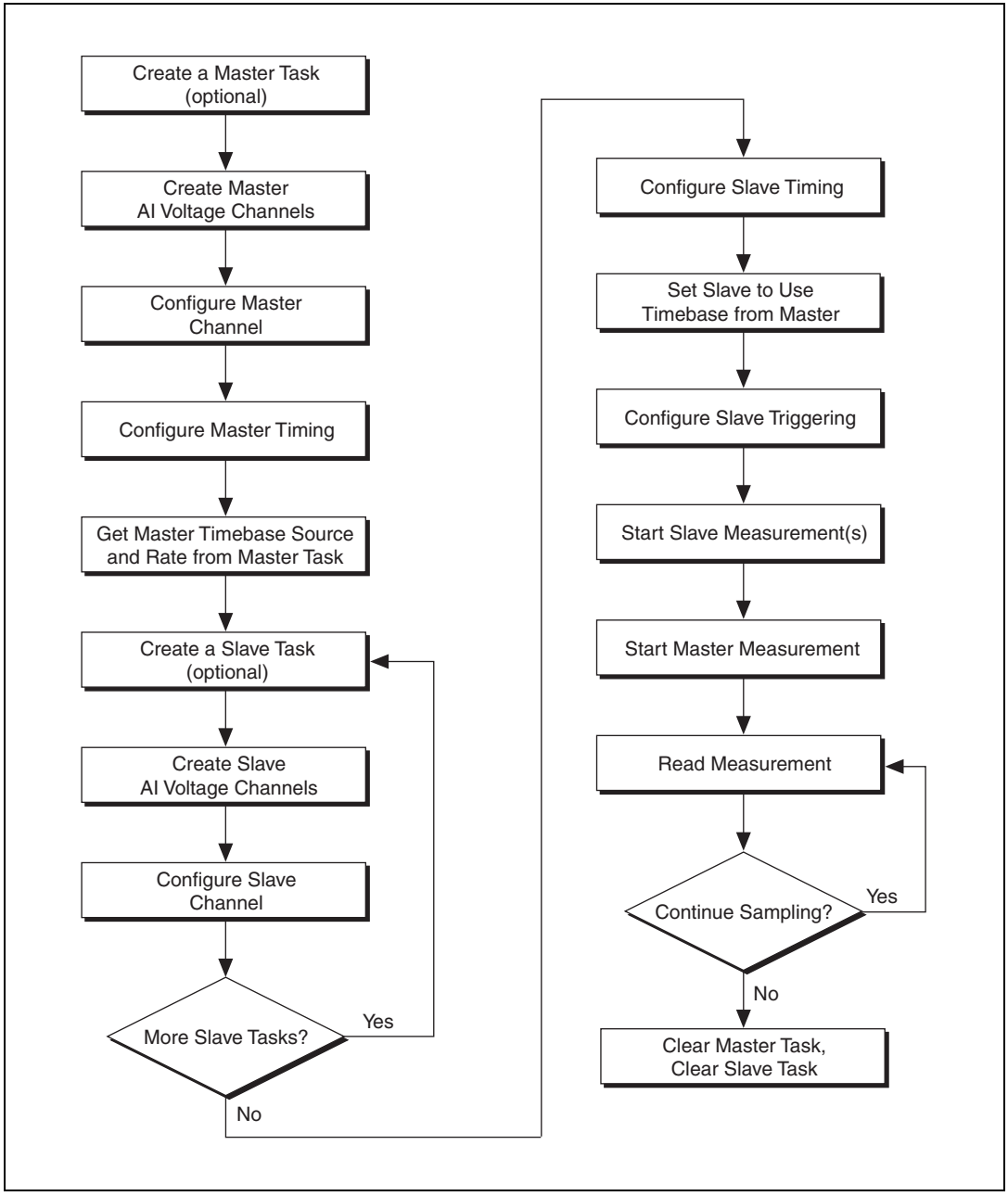


Figure 5-2. General Synchronizing Flowchart

Synchronizing the NI PXI-4224/4225 Using LabVIEW

This section describes in more detail the steps shown in Figure 5-2, *General Synchronizing Flowchart*, such as how to create a task in LabVIEW and configure the channels of the NI PXI-4224/4225. For further instructions, select **Help»VI, Function, & How-To Help** from the LabVIEW menu bar.

Note Except where otherwise stated, the VIs in Table 5-3 are located on the **Functions» All Functions»NI Measurements»DAQmx - Data Acquisition** subpalette and accompanying subpalettes in LabVIEW.

Table 5-3. Synchronizing the NI PXI-4224/4225 Using LabVIEW

Flowchart Step	VI or Program Step
Create a Master Task (optional)	`DAQmx Create Task.vi`—This VI is optional if you created and configured your task using the DAQ Assistant. However, if you use it in LabVIEW, any changes you make to the task will not be saved to a task in MAX.
Create Master AI Voltage Channels	`DAQmx Create Virtual Channel.vi` (AI Voltage by default).
Configure Master Channels	Use a DAQmx Channel Property Node. Refer to the *Using a DAQmx Channel Property Node in LabVIEW* section for more information.
Configure Master Timing	`DAQmx Timing.vi` (Sample Clock by default).
Get Master Timebase Source and Rate from Master Task	Use a DAQmx Timing Property Node to get `MasterTimebase.Src` and `MasterTimebase.Rate`.
Create a Slave Task (optional)	`DAQmx CreateTask.vi`—This VI is optional if you created and configured your task using the DAQ Assistant. However, if you use it in LabVIEW, any changes you make to the task will not be saved to a task in MAX.
Create Slave AI Voltage Channels	`DAQmx Create Virtual Channel.vi` (AI Voltage by default).
Configure Slave Channels	DAQmx Channel Property Node. Refer to the *Using a DAQmx Channel Property Node in LabVIEW* section for more information.
Configure Slave Timing	`DAQmx Timing.vi` (Sample Clock by default).

Table 5-3. Synchronizing the NI PXI-4224/4225 Using LabVIEW (Continued)

Flowchart Step	VI or Program Step
Set Slave to Use Timebase from Master	Use a DAQmx Timing Property Node to set `MasterTimebase.Src` and `MasterTimebase.Rate` to the values retrieved from the master task in the *Get Master Timebase Source and Rate from Master Task* step.
Configure Slave Triggering	`DAQmx Trigger.vi` (Start Digital Edge) use `/MasterDevice/ai/StartTrigger` as the source, substituting the master device identifier for `MasterDevice`.
Start Slave Measurement(s)	`DAQmx Start Task.vi`
Start Master Measurement	`DAQmx Start Task.vi`
Read Measurement	`DAQmx Read.vi`
Continue Sampling	For continuous sampling, use a While Loop. You also need to set the sample mode to **Continuous Samples** in the *Configure Master Timing* and *Configure Slave Timing* steps. To do this, right-click the terminal of the `DAQmx Timing.vi` labeled **sample mode** and click **Create»Constant**. Click the checkbox and select **Continuous Samples**.
Clear Master Task	`DAQmx Clear Task.vi`
Clear Slave Task	`DAQmx Clear Task.vi`

Other Application Documentation and Material

The following locations provide more information that you may find useful when setting up or connecting signal sources or programming your application.

- LabVIEW Example Programs, available by selecting **Open» Examples** from the opening screen. Most of the examples applicable to the NI PXI-4224/4225 are located in **Hardware Input and Output»DAQmx»Analog Measurements** and **Hardware Input and Output»DAQmx»Synchronization»Multi-Device**.
- *PXI-4225 Supported Properties* and *PXI-4224 Supported Properties* in the LabVIEW *VI, Function, & How-To Help*.
- Application Note 025: *Field Wiring and Noise Considerations for Analog Signals* available at `ni.com/info` using the info code `rdfwn3`.

Calibrating the NI PXI-4224/4225

Calibration refers to the process of minimizing measurement errors. On the NI PXI-4224/4225, errors from the digitizer components of the DAQ device circuitry are corrected in the analog circuitry by onboard calibration digital-to-analog converters (CalDACs). Errors from the signal conditioning circuitry are corrected in software.

Three levels of calibration are available for the NI PXI-4224/4225 to ensure the accuracy of its analog circuitry. The first level, loading calibration constants, is the fastest, easiest, and least accurate. The NI PXI-4224/4225 automatically loads calibration constants stored in flash memory when powered on. The intermediate level, internal calibration, is the preferred method for assuring accuracy in your application. The last level, external calibration, is the slowest, most difficult, and most accurate.

Loading Calibration Constants

The NI PXI-4224/4225 is factory calibrated before shipment at approximately 25 °C to the levels indicated in Appendix A, *Specifications*. The associated calibration constants are stored in the onboard nonvolatile flash memory. These constants are the values that were written to the CalDACs to achieve calibration in the factory and the remaining signal conditioning error. The digitizer calibration constants are automatically read from the flash memory and loaded into the CalDACs by the NI PXI-4224/4225 hardware the next time the device driver software is loaded. The signal conditioning calibration constants are also read from the flash memory at this time.

Self-Calibration

The NI PXI-4224/4225 can measure and correct for most of its calibration-related errors without any external signal connections. This calibration method is referred to as internal calibration or self-calibration. This internal calibration process, which generally takes less than two minutes, is the preferred method for assuring accuracy in your application. Initiate an internal calibration to minimize the effects of any offset and gain drifts, particularly those due to changes in temperature. During the internal calibration process, the AI channels are compared to the NI PXI-4225/42224 onboard voltage reference. The majority of the

offset and gain errors in the analog circuitry are compensated for by adjusting the CalDACs to minimize these errors. To perform a self-calibration, complete the following steps:

1. Double-click the **Measurement & Automation Explorer** icon on the desktop.
2. Expand **Devices and Interfaces** to display the list of devices and interfaces.
3. Expand **NI-DAQmx Devices** to display the list of NI-DAQmx devices.
4. Right-click the NI PXI-4225 or NI PXI-4224 and select **Self-Calibrate**.
5. A dialog box opens indicating that the NI PXI-4225 or NI PXI-4224 is self-calibrating.
6. When the dialog box closes, the NI PXI-4224/4225 is successfully self-calibrated.

Note The NI PXI-4224/4225 also can be self-calibrated programmatically by using `DAQmx Self Calibrate.vi` in LabVIEW.

The results of an internal calibration are stored in the NI PXI-4224/4225 flash memory so that the CalDACs are automatically loaded with the newly calculated calibration constants the next time the NI PXI-4224/4225 is powered on.

Performing a self-calibration at the operating temperature of your application will ensure the NI PXI-4224/4225 meets the specifications in Appendix A, *Specifications*.

External Calibration

You can download all available external calibration documents by going to `ni.com/calibration` and clicking **Manual Calibration Procedures**. NI recommends you perform an external calibration once a year.

A

Specifications

This appendix lists the specifications for both the NI PXI-4225 and NI PXI-4224 device unless otherwise noted. These specifications are typical at 25 °C unless otherwise noted.

Overvoltage Protection

Powered on or off

NI PXI-4225 ..... 150 V max

NI PXI-4224 ..... 42.4 V_{peak} max

SMB connector ..... ±15 V, powered on or off

Analog Input

Number of input channels 8

Input range ..... ±10 VDC

Resolution ..... 16 bits

Maximum sampling rate.....200 kS/s aggregate multichannel

Table A-1. Maximum Sampling Rates

Number of Channels	Sample Rate
1	333 kS/s/ch
2	100.0 kS/s/ch
3	66.6 kS/s/ch
4	50.0 kS/s/ch
5	40.0 kS/s/ch
6	33.3 kS/s/ch
7	28.5 kS/s/ch
8	25.0 kS/s/ch

Input coupling.....DC

Bandwidth

50/60 Hz selectable line filter.....10 Hz, –3 dB
(PXI-4225 only)

10 kHz selectable, 3rd minimum.....10 kHz, –3 dB
(PXI-4225 only)

Filter bypass.....30 kHz, –3 dB

Slew rate .....2 Vμs typical

Input impedance

Powered on .....100 MΩ parallel 100 pF

Powered off .....30 kΩ

Input bias current .....100 pA typ
600 pA max

NMR, 10 Hz filter enabled .....40 dB at 50 Hz typ
45 dB at 60 Hz typ
(both NI PXI-4225 only)

Offset error

Gain	Offset Temperature Coefficient (μV/°C) max	Gain Temperature Coefficient (ppm/°C) max
1	224	15
2	115	18
5	51.5	19
10	26.2	20
20	15.8	22
50	9.6	24
100	7.55	24
200	6.52	24
500	5.91	24
1000	5.71	25
Note: The NI-PXI-4224 has gains of 1 and 10 only.		

CMRR ..... 130 db at DC 60 Hz, balanced, typ

100 dB at DC 60 Hz,
10 kΩ imbalanced, typ

70 dB at DC 60 Hz to 10 kHz,
10 kΩ imbalanced, min

Crosstalk at 1 kHz

Adjacent channels ..... –75 dB typ

All other channels ..... –90 dB typ

FIFO buffer size ..... 512 samples

Data transfers ..... DMA, interrupts, programmed I/O

DMA modes ..... Scatter-gather (single transfer, demand transfer)

Configuration memory size ..... 512 words

NI PXI-4224/4225 Accuracy Information

Nominal Range (V)	Absolute Accuracy					Absolute Accuracy at Full Scale (mV)	Relative Accuracy Resolution (µV)	
	% of Reading 1 Year	Offset (mV)	Noise + Quantization (mV)		Temp Drift (%/°C)		Single Point	Averaged
			Single Pt.	Avg.				
±10 V	0.034	±2710	±859	±82.0	0.0020	6.19	305	108
±5 V	0.036	±1372	±640	±62.7	0.0023	3.23	153	54.2
±2 V	0.036	±575	±557	±55.5	0.0024	1.35	61	21.7
±1 V	0.037	±290	±131	±12.8	0.0025	0.67	31	10.8
±0.5 V	0.038	±158	±118	±11.7	0.0027	0.36	15	5.42
±0.2 V	0.039	±79.8	±113	±11.3	0.0029	0.17	6.1	2.17
±0.1 V	0.039	±53.6	±113	±11.3	0.0029	0.10	3.1	1.08
±0.05 V	0.039	±40.6	±112	±11.2	0.0029	0.07	1.5	0.542
±0.02 V	0.039	±32.7	±112	±11.2	0.0029	0.05	0.61	0.217
±0.01 V	0.039	±30.1	±111	±11.1	0.0029	0.05	0.31	0.108

Accuracies are valid for measurements following an internal self-calibration. Averaged numbers assume dithering and averaging of 100 single-channel readings.

Measurement accuracies are listed for operational temperatures within ±5 °C of internal calibration temperature and ±10 °C of external or factory calibration temperature.

Transfer Characteristics

Nonlinearity .....0.02% FSR typ

DNL .....±0.5 LSB typ, ±1 LSB max

No missing codes.....16 bits, guaranteed

Calibration

Recommended warm-up time.....15 minutes

External calibration interval .....1 year

Onboard calibration reference

Level.....5.000 V ±1 mV (actual value stored in EEPROM)

TC.....±5 ppm/°C

Long-term stability .....15 ppm/$\sqrt{1000h}$

Pre-Calibration Errors[1]

Pre-calibration offset error relative to input (RTI) ..... 865 mV max

Signal conditioning component only..... ±50 mV typ, ±160 mV max at a gain of 1

Pre-calibration gain error ..... ±18,900 ppm max

Signal conditioning component only..... ±600 ppm typ, ±1,000 ppm max at a gain of 1

Digital Triggers

Number of triggers 2

Purpose..... Start and stop trigger, gate, clock

Source..... PFI0/AI START TRIG (front SMB connector), PXI_TRIG<0..5> to PXI_Star (PXI trigger bus)

Compatibility ..... 5 V/TTL

Response ..... Rising or falling edge

Pulse width..... 10 ns min

Impedance ..... 10 kΩ

Coupling..... DC

PXI Trigger Bus

Trigger lines 6

Star trigger..... 1

PCI Bus Interface

Master, slave

[1] The pre-calibration errors apply only to users doing register level programming. Pre-calibration errors are not visible to NI-DAQmx users.

Power Requirements

2 A at +5 VDC (±5%)

Physical

Dimensions (not including connectors).....16.0 × 10.0 × 2.0 cm (6.3 × 3.9 in.)

Analog input signal connector.....25-Pin D-SUB

Maximum Working Voltage

PXI-4225

(Signal + common-mode) each input should remain within ±150 V of ground.

Maximum working voltage refers to the signal voltage plus the CMV.

Channel-to-earth (inputs).....150 V_{rms} or VDC, Installation Category II

Channel-to-channel (inputs) .....150 V_{rms} or VDC, Installation Category II

Cautions This device is rated for Installation Category II and is intended to carry signal voltages no greater than 150 V. Do *not* connect to MAINS supply circuits greater than 150 VAC (for example wall outlets) of 230 VAC. This device can withstand up to 800V impulse, from inputs to earth and channel-to-channel, and up to 1,500 V impulse from inputs to PXI Bus without creating a safety hazard. Do not use this device for connection to signals or for measurements within Categories III or IV.

When hazardous voltages (> 42.4 V_{pk}/60 VDC) are present on any channel, safety low-voltage (< 42.4 V_{pk}/60 VDC) cannot be connected to any other channel.

PXI-4224

(Signal + common-mode) each input should remain within 42.4 V_{peak} of ground.

Maximum working voltage refers to the signal voltage plus the CMV.

Channel-to-earth (inputs) ..... 42.4 V_{peak} or VDC, Installation Category I

Channel-to-channel (inputs)..... 42.4 V_{peak} or VDC, Installation Category I

Caution This device is rated for Installation Category I and is intended to carry signal voltages no greater than 42 V. This device can withstand up to 400 V impulse voltage without creating a safety hazard. Do not use this device for connection to signals or for measurements within Categories II, III, or IV.

Environmental

Operating temperature..... 0 to 55 °C

Storage temperature ..... –20 to 70 °C

Humidity ..... 10 to 90% RH, noncondensing

Maximum altitude ..... 2,000 m

Pollution Degree (indoor use only) 2

Safety

The PXI-4224/4225 is designed to meet the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1
- CAN/CSA-C22.2 No 61010-1

Note For UL and other safety certifications, refer to the product label, or visit `ni.com/certification`, search by model number or product line, and click the appropriate link in the Certification column.

Electromagnetic Compatibility

Emissions.....EN 55011 Class A at 10 m
FCC Part 15A above 1 GHz

Immunity .....EN 61326:1997 + A2:2001, Table 1

EMC/EMI .....CE, C-Tick, and FCC Part 15 (Class A) Compliant

Note For EMC compliance, operate this device with shielded cabling.

CE Compliance

The PXI-4224/4225 meets the essential requirements of applicable European Directives, as amended for CE marking, as follows:

Low-Voltage Directive (safety).....73/23/EEC

Electromagnetic Compatibility Directive (EMC).....89/336/EEC

Note Refer to the Declaration of Conformity (DoC) for this product for any additional regulatory compliance information. To obtain the DoC for this product, visit `ni.com/certification`, search by model number or product line, and click the appropriate link in the Certification column.

B

Timing Signal Information

This appendix contains additional information about the timing signals discussed in Chapter 4, *Theory of Operation*.

Connecting Timing Signals

Caution Exceeding the maximum input voltage ratings listed in Appendix A, *Specifications*, can damage the device and the computer. NI is *not* liable for any damage resulting from such signal connections.

Programmable Function Input Connections

You can externally control seven internal timing signals from PFI0 and the PXI trigger bus pins. The source for each of these signals is software configurable from PFI0, PXI_Trig<0..5>, or PXI_Star when you want external control. This flexible routing scheme reduces the need to change the physical wiring to the device I/O connector for applications requiring alternative wiring.

As an input, each PFI signal can be individually configured for edge or level detection and polarity selection. You can use the polarity selection for any timing signal, but the edge or level detection depends on the particular timing signal being controlled. The detection requirements for each timing signal are listed in the corresponding sections.

In edge-detection mode, the minimum pulse width required is 10 ns. This requirement applies for both rising-edge and falling-edge polarity settings. There is no maximum pulse width requirement in edge-detection mode.

In level-detection mode, there are no pulse width requirements imposed by the PFIs themselves. Limits can be imposed by the particular timing signal being controlled. These requirements are listed in the sections that describe the signals.

DAQ Timing Connections

The timing signals are AI START TRIG, AI REF TRIG, AI SAMP CLK, AI CONV CLK, AI PAUSE TRIG, AI SAMPLE CLK TIMEBASE, and AI HOLD COMPLETE.

Posttriggered DAQ allows you to view data that is acquired after a trigger event is received. Figure B-1 shows a typical posttriggered sequence.

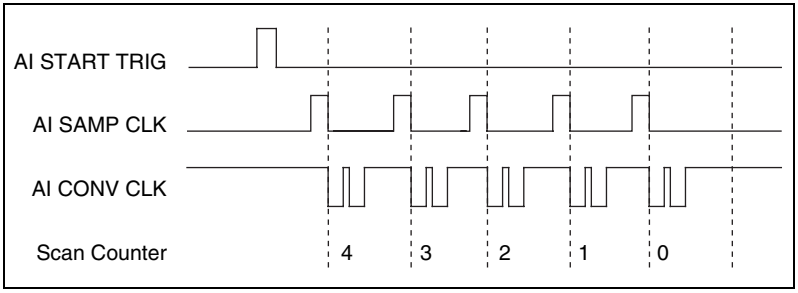


Figure B-1. Typical Posttriggered Sequence

Pretriggered DAQ allows you to view data that is acquired before the trigger of interest in addition to data acquired after the trigger. Figure B-2 shows a typical pretriggered sequence.

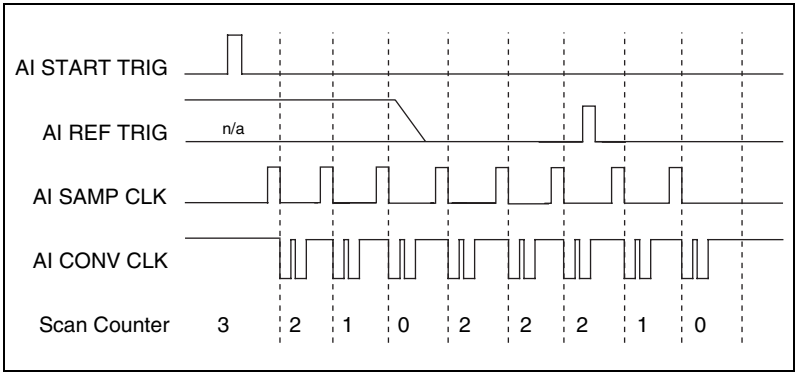


Figure B-2. Typical Pretriggered Sequence

AI START TRIG Signal

The AI START TRIG signal can be input or output through PFI0, PXI_Trig<0..5>, or PXI_Star.

As an input, AI START TRIG is configured in the edge-detection mode. You can select PFI0 as the source for AI START TRIG and configure the

polarity selection for either rising or falling edge. The selected edge of AI START TRIG starts the sequence for both posttriggered and pretriggered acquisitions. Refer to Figures B-1 and B-2 for the relationship of AI START TRIG to the sequence.

As an output, AI START TRIG reflects the action that initiates a sequence, even if the acquisition is externally triggered by another PFI. The output is an active high pulse with a pulse width of 50 to 100 ns. This output is set to high-impedance at startup.

Figures B-3 and B-4 show the input and output timing requirements for AI START TRIG.

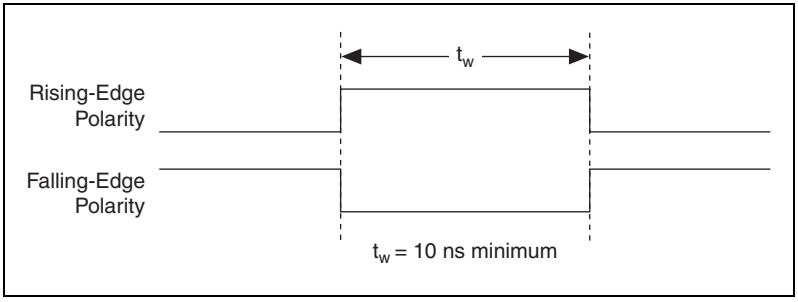


Figure B-3. IAI START TRIG Input Signal Timing

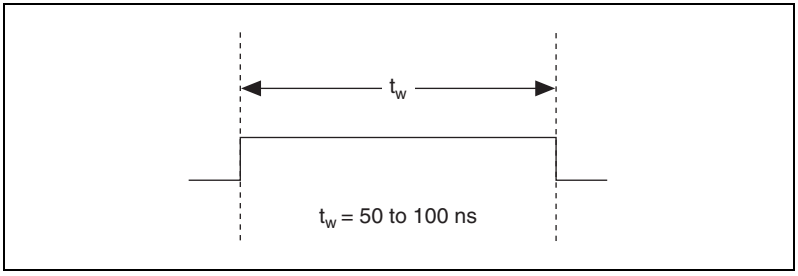


Figure B-4. AI START TRIG Output Signal Timing

The device also uses AI START TRIG to initiate pretriggered operations. In pretriggered applications, AI START TRIG is generated by a software trigger unless a PFI pin is selected as the source of AI START TRIG. Refer to the *AI REF TRIG Signal* section for a complete description of the use of AI START TRIG and AI REF TRIG in a pretriggered operation.

AI REF TRIG Signal

The AI REF TRIG signal can be input through PFI0, PXI_Trig<0..5>, or PXI_Star. Refer to Figure B-2 for the relationship of AI REF TRIG to the sequence.

As an input, AI REF TRIG is configured in edge-detection mode. You can configure the polarity selection for either rising or falling edge. The selected edge of AI REF TRIG initiates the posttriggered phase of a pretriggered sequence. In pretriggered mode, the AI START TRIG signal initiates the acquisition. The scan counter (SC) indicates the minimum number of scans before AI REF TRIG is recognized. After the SC decrements to zero, it is loaded with the number of posttrigger scans to acquire while the acquisition continues. The device ignores AI REF TRIG if it is asserted prior to the SC decrementing to zero. After the selected edge of AI REF TRIG is received, the device acquires a fixed number of scans and the acquisition stops. In pretriggered mode, the device acquires data both before and after receiving AI REF TRIG.

As an output, AI REF TRIG reflects the posttrigger in a pretriggered sequence, even if the acquisition is externally triggered by another PFI. AI REF TRIG is not used in posttriggered DAQ. The output is an active high pulse with a pulse width of 50 to 100 ns. This output is set to high-impedance at startup.

Figures B-5 and B-6 show the input and output timing requirements for AI REF TRIG.

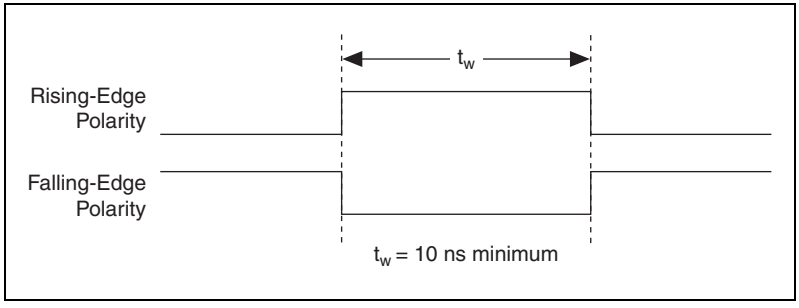


Figure B-5. AI REF TRIG Input Signal Timing

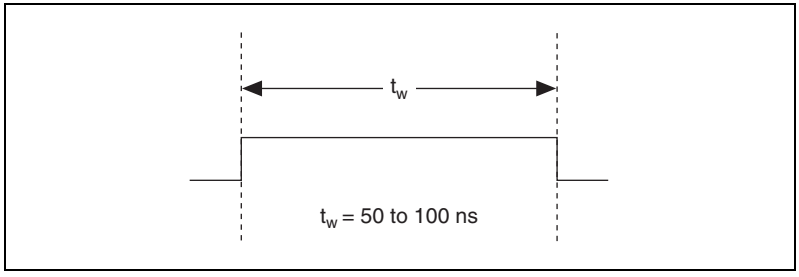


Figure B-6. AI REF TRIG Output Signal Timing

AI SAMP CLK Signal

The AI SAMP CLK signal can be externally input from PFI0, PXI_Trig<0..5>, or PXI_Star. It can be output on any PXI trigger bus line. Refer to Figures B-1 and B-2 for the relationship of AI SAMP CLK to the sequence.

As an input, AI SAMP CLK is configured in edge-detection mode. You can configure the polarity selection for either rising or falling edge.
The selected edge of AI SAMP CLK initiates a scan. The SI2 counter starts if you select an internally triggered AI CONV CLK.

As an output, AI SAMP CLK reflects the actual start pulse that initiates a scan, even if the starts are externally triggered by another PFI or PXI_Trig<0..5>. Two output options are available. The first option is an active high pulse with a pulse width of 50 to 100 ns, which indicates the start of the scan. The second option is an active high pulse that terminates at the start of the last conversion in the scan, which indicates a scan in progress. AI SAMP CLK is deasserted, t_{off}, after the last conversion in the scan is initiated. This output is set to high-impedance at startup.

Figures B-7 and B-8 show the input and output timing requirements for AI SAMP CLK.

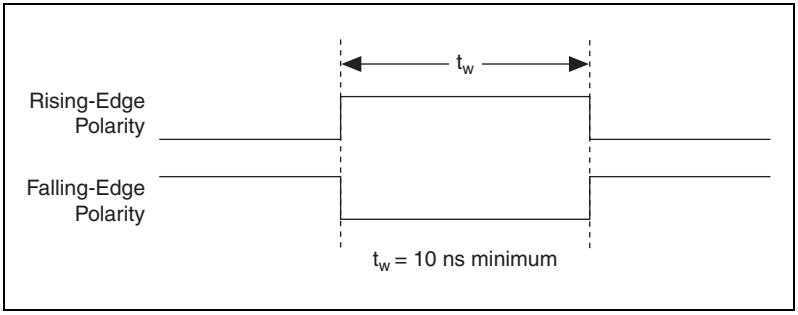


Figure B-7. AI SAMP CLK Input Signal Timing

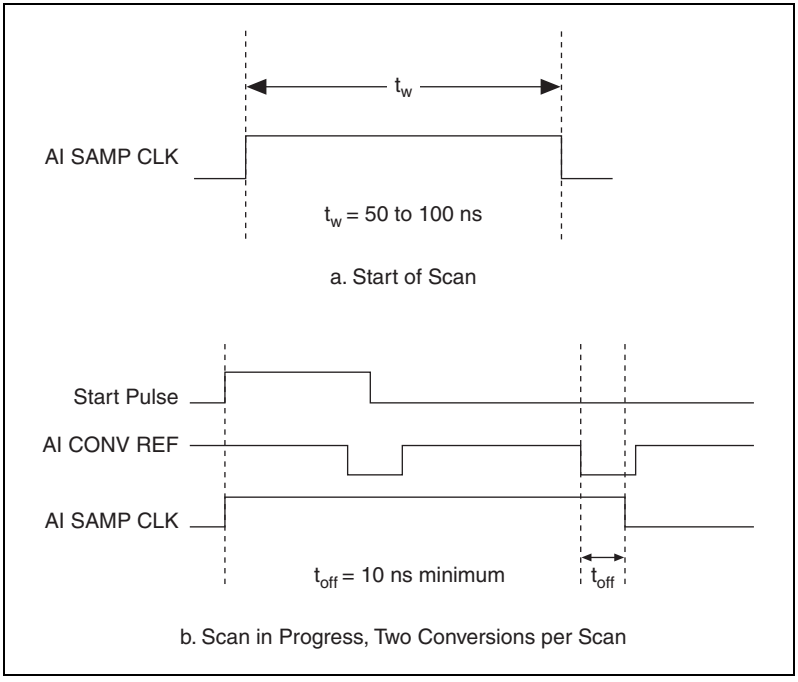


Figure B-8. AI SAMP CLK Output Signal Timing

The AI CONV CLK pulses are masked off until the device generates AI SAMP CLK. If you use internally generated conversions, the first AI CONV CLK appears when the onboard SI2 counter reaches zero. If you select an external AI CONV CLK, the first external pulse after AI SAMP CLK generates a conversion. Separate the AI SAMP CLK pulses by at least one scan period.

A counter on the device internally generates AI SAMP CLK unless you select some external source. The AI START TRIG signal starts this counter, and the application software or the sample counter stops it.

Scans generated by either an internal or external AI SAMP CLK are inhibited unless they occur within a sequence. Scans occurring within a sequence can be gated by either the hardware AI PAUSE TRIG signal or the software command register gate.

AI CONV CLK Signal

PFI0, PXI_Trig<0..5>, or PXI_Star can externally input the AI CONV CLK signal, which is also available as an output on PXI_Trig<0..5> or PXI_Star.

Refer to Figures B-1 and B-2 for the relationship of AI CONV CLK to the sequence.

As an input, AI CONV CLK is configured in edge-detection mode. You can configure the polarity selection for either rising or falling edge. The selected edge of AI CONV CLK initiates an A/D conversion.

As an output, AI CONV CLK reflects the actual convert pulse that connects to the ADC, even if the conversions are externally generated by another PFI. The output is an active low pulse with a pulse width of 50 to 100 ns. This output is set to high-impedance at startup.

Figures B-9 and B-10 show the input and output timing requirements for AI CONV CLK.

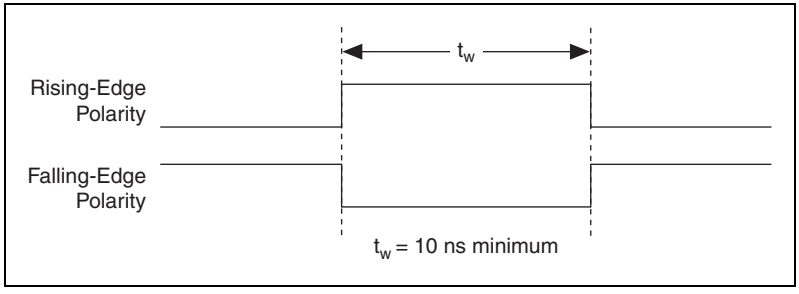


Figure B-9. AI CONV CLK Input Signal Timing

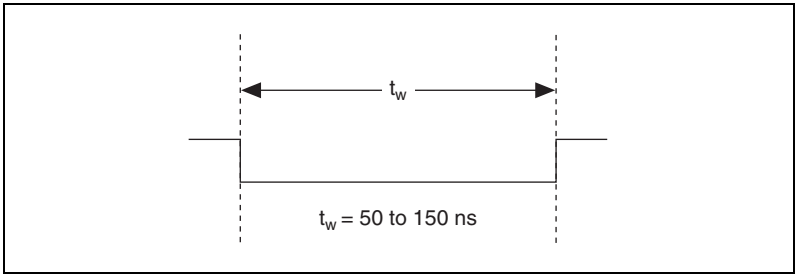


Figure B-10. AI CONV CLK Output Signal Timing

The ADC switches to hold mode within 60 ns of the selected edge. This hold-mode delay time is a function of temperature and does not vary from one conversion to the next. Separate the AI CONV CLK pulses by at least one conversion period.

The NI PXI-4224/4225 sample interval counter generates AI CONV CLK unless you select an external source. The AI SAMP CLK signal starts the counter, which counts down and reloads itself until the scan finishes. The counter then reloads itself in preparation for the next AI SAMP CLK pulse.

A/D conversions generated by an internal or external AI CONV CLK signal are inhibited unless they occur within a sequence. Scans occurring within a sequence can be gated by either the hardware AI PAUSE TRIG signal or the software command register gate.

AI PAUSE TRIG Signal

PFI0, PXI_Trig<0..5>, or PXI_Star can externally input the AI PAUSE TRIG signal, which is not available as an output on the I/O connector. AI PAUSE TRIG can mask off scans in a sequence. You can configure the pin you select as the source for AI PAUSE TRIG in level-detection mode. You can configure the polarity selection for the pin as either active high or active low.

In level-detection mode, the AI SAMP CLK signal is masked off and no scans can occur.

AI PAUSE TRIG can neither stop a scan in progress nor continue a previously gated-off scan. In other words, once a scan has started, AI PAUSE TRIG does not gate off conversions until the beginning of the next scan. Conversely, if conversions are gated off, AI PAUSE TRIG does not gate them back on until the beginning of the next scan.

AI SAMPLE CLK TIMEBASE Signal

PFI0, PXI_Trig<0..5>, or PXI_Star can externally input the AI SAMPLE CLK TIMEBASE signal, which is not available as an output on the I/O connector. The onboard scan interval (SI) counter uses AI SAMPLE CLK TIMEBASE as a clock to time the generation of the AI SAMP CLK signal. Configure the pin you select as the source for AI SAMPLE CLK TIMEBASE in level-detection mode. Configure the polarity selection for the pin for either active high or active low.

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 23 ns high or low. There is no minimum frequency.

Either the 20 MHz or 100 kHz internal timebase generates AI SAMPLE CLK TIMEBASE unless you select an external source. Figure B-11 shows the timing requirements for AI SAMPLE CLK TIMEBASE.

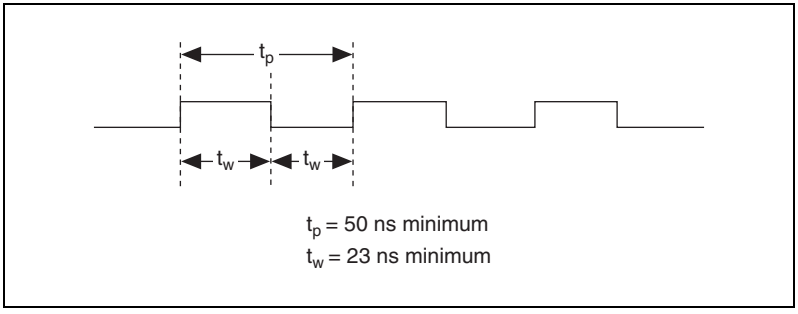


Figure B-11. AI SAMPLE CLK TIMEBASE Signal Timing

AI HOLD COMPLETE Signal

AI HOLD COMPLETE is an output-only signal that generates a pulse with the leading edge occurring approximately 50 to 100 ns after an A/D conversion begins. The polarity of this output is software configurable, but the polarity is typically configured so that a low-to-high leading edge can clock external analog input multiplexers that indicate when the input signal has been sampled and can be removed. This signal has a 400 to 500 ns pulse width and is software enabled. Figure B-12 shows the timing for AI HOLD COMPLETE.

Note The polarity of AI HOLD COMPLETE is not software selectable when programmed using NI-DAQmx. It is a positive polarity pulse.

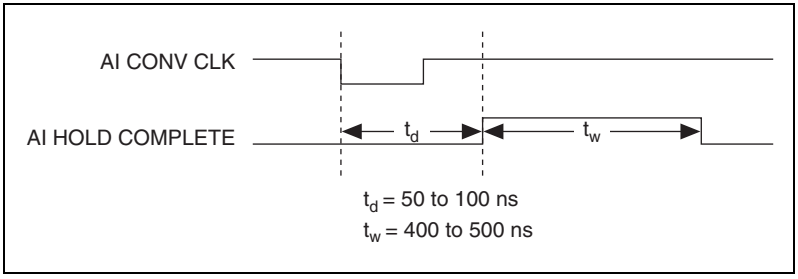


Figure B-12. AI HOLD COMPLETE Signal Timing

C

Removing the NI PXI-4224/4225

This section provides details for removing an NI PXI-4224/4225 device from MAX and from a PXI or PXI/SCXI combination chassis.

Note You must physically remove the NI PXI-4224/4225 from the chassis before you can remove it from MAX.

Removing the NI PXI-4224/4225 from a PXI or PXI/SCXI Combination Chassis

Consult the PXI or PXI/SCXI chassis documentation for additional instructions and cautions. To remove the NI PXI-4224/4225 device from a PXI or PXI/SCXI chassis, complete the following steps while referring to Figure C-1:

1. Power off the PXI chassis. Do *not* remove the NI PXI-4224/4225 device from a chassis that is powered on. If the you are using a PXI/SCXI combination chassis, also power off the SCXI portion of the chassis
2. Rotate the mounting screws that secure the NI PXI-4224/4225 to the chassis counter-clockwise until they are loose, but do not completely remove the screws.
3. Remove the NI PXI-4224/4225 by pushing down steadily on the injector/ejector handle until the device disengages from the chassis.
4. Slide the device completely out.

The next time you restart the computer the NI PXI-4224/4225 will have a red circle with a white **X** inside it next to the device in MAX.

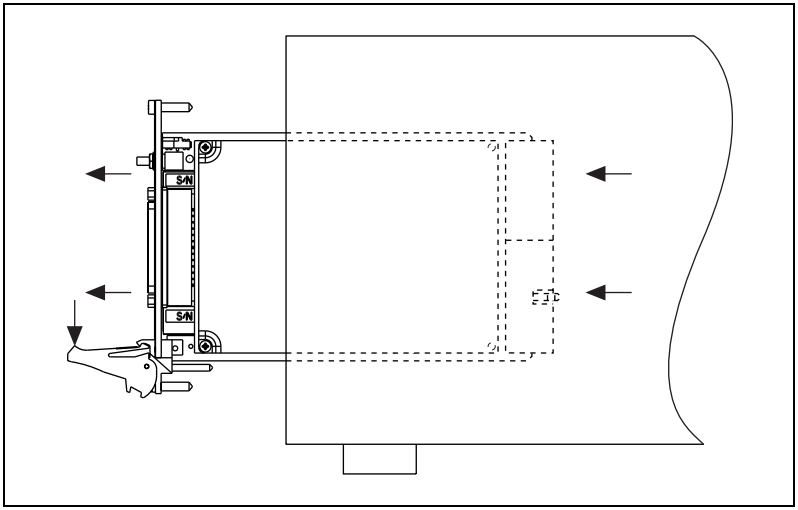


Figure C-1. Injector/Ejector Handle Position Before Device Removal

Removing the NI PXI-4224/4225 from MAX

To remove an NI PXI-4224/4225 device from MAX, complete the following steps after launching MAX:

1. Expand **Devices and Interfaces** to display the list of installed devices and interfaces. The NI PXI-4225 or NI PXI-4224 should have a red circle with a white **X** inside it next to the device to indicate it has been physically removed from the chassis.
2. Right-click the NI PXI-4224/4225 and click **Delete**.
3. You are presented with a confirmation window. Click **Yes** to continue deleting the device or **No** to cancel this action.

The NI PXI-4224/4225 is now removed from the list of installed devices in MAX.

D

Common Questions

This appendix lists common questions related to the use of the NI PXI-4224/4225.

Which version of NI-DAQ works with the NI PXI-4224/4225 and how do I get the most current version of NI-DAQ?

You must have NI-DAQ 7.3.1 or later and use NI-DAQmx.

1. Go to `ni.com`.
2. Follow the link, **Download Software»Drivers and Updates»Search Drivers and Updates**.
3. Enter the keyword `NI-DAQ` to find the latest version of NI-DAQ for your operating system.

Does the NI PXI-4224/4225 have hardware analog triggering?

No.

Is the NI PXI-4224/4225 an isolated device?

Yes, the NI PXI-4224/4225 provides true channel-to-channel and channel-to-chassis isolation.

When no signal is connected to the NI PXI-4224/4225, what behavior should I expect?

While the NI PXI-4224/4225 may react differently because of system and condition variables, in most cases, a channel drifts to one extreme output. To prevent this behavior short the inputs to unused channels.

How do I program the NI PXI-4224/4225?

Refer to Chapter 4, *Theory of Operation*, or your ADE help file for application programming information. There is no register-level programming manual available for the NI PXI-4224/4225.

How do I perform an external calibration of the NI PXI-4224/4225?

As of the NI PXI-4224/4225 release, an external calibration document is not available. To check the availability of an NI PXI-4224/4225 external calibration document is go to `ni.com/calibration` and click **Manual Calibration Procedures**.

Glossary

Symbol	Prefix	Value
p	pico	10^{-12}
n	nano	10^{-9}
μ	micro	10^{-6}
m	milli	10^{-3}
k	kilo	10^{3}
M	mega	10^{6}
G	giga	10^{9}
T	tera	10^{12}

Numbers/Symbols

%	Percent.
+	Positive of, or plus.
–	Negative of, or minus.
/	Per.
°	Degree.
Ω	Ohm.

A

A	Amperes.
A/D	Analog-to-digital.
AC	Aternating current.

ADC	Analog-to-digital converter—An electronic device, often an integrated circuit, that converts an analog voltage to a digital number.
ADE	Application development environment.
AI	Analog input.
AI CONV CLK	Convert signal.
AI HOLD COMPLETE	Scan clock signal.
AI PAUSE TRIG	Analog input gate signal.
AI SAMP CLK	Start scan signal.

B

bandwidth	The range of frequencies present in a signal, or the range of frequencies to which a measuring device can respond.
bipolar	A signal range that includes both positive and negative values (for example, –5 to +5 V).
breakdown voltage	The voltage high enough to cause breakdown of optical isolation, semiconductors, or dielectric materials. *See* working voltage.
bus	The group of conductors that interconnect individual circuitry in a computer. Typically, a bus is the expansion vehicle to which I/O or other devices are connected. An example of a PC bus is the PCI bus.

C

C	Celsius.
CalDAC	Calibration DAC.
CH	Channel—Pin or wire lead to which you apply or from which you read the analog or digital signal. Analog signals can be single-ended or differential. For digital signals, you group channels to form ports. Ports usually consist of either four or eight digital channels.
channel clock	The clock controlling the time interval between individual channel sampling within a scan.

CMR	Common-mode rejection.
CMRR	Common-mode rejection ratio—A measure of an instrument's ability to reject interference from a common-mode signal, usually expressed in decibels (dB).
common-mode signal	Any voltage present at the instrumentation amplifier inputs with respect to amplifier ground.
counter/timer	A circuit that counts external pulses or clock pulses (timing).

D

D/A	Digital-to-analog.
DAC	Digital-to-analog converter—An electronic device, often an integrated circuit, that converts a digital number into a corresponding analog voltage or current.
DAQ	Data acquisition—(1) Collecting and measuring electrical signals from sensors, transducers, and test probes or fixtures and inputting them to a computer for processing; (2) collecting and measuring the same kinds of electrical signals with A/D and/or DIO devices plugged into a computer, and possibly generating control signals with D/A and/or DIO devices in the same computer.
DAQ Assistant	A configuration assistant with which you define and configure your DAQ operation.
DAQ-STC	Data acquisition system timing controller chip.
dB	Decibel—The unit for expressing a logarithmic measure of the ratio of two signal levels: $db = 20 \cdot \log_{10}(V1/V2)$, for signals in volts.
DC	Direct current.
D GND	Digital ground signal.
differential input	An analog input consisting of two terminals, both of which are isolated from computer ground, whose difference is measured.
DIO	Digital input/output.
dithering	The addition of Gaussian noise to an analog input signal.

DMA	Direct memory access—A method by which data can be transferred to/from computer memory from/to a device or memory on the bus while the processor does something else. DMA is the fastest method of transferring data to/from computer memory.
DNL	Differential nonlinearity—A measure in least significant bit of the worst-case deviation of code widths from their ideal value of 1 LSB.
driver	Software that controls a specific hardware device such as a DAQ device.

E

EEPROM	Electrically erasable programmable read-only memory—ROM that can be erased with an electrical signal and reprogrammed.
EMC	Electromagnetic compatibility.
EMI	Electromagnetic interference—Defines unwanted electromagnetic radiation from a device, which could interfere with desired signals in test or communication equipment.
ESD	Electrostatic discharge.

F

FIFO	First-in first-out memory buffer.
floating signal sources	Signal sources with voltage signals that are not connected to an absolute reference or system ground. Also called nonreferenced signal sources. Some common example of floating signal sources are batteries, transformers, or thermocouples.

G

g	Gram or grams.
gain	The factor by which a signal is amplified, sometimes expressed in decibels.
gain accuracy	A measure of deviation of the gain of an amplifier from the ideal gain.

H

h	Hour or hours.
Hz	Hertz—The number of scans read or updates written per second.

I

I/O	Input/output—The transfer of data to/from a computer system involving communications channels, operator interface devices, and/or DAQ and control interfaces.
in.	Inch or inches.
INL	Integral nonlinearity—A measure in LSB of the worst-case deviation from the ideal A/D or D/A transfer characteristic of the analog I/O circuitry.
input bias current	The current that flows into the inputs of a circuit.
input impedance	The resistance and capacitance between the input terminals of a circuit.
input offset current	The difference in the input bias currents of the two inputs of an instrumentation amplifier.
instrumentation amplifier	A circuit whose output voltage with respect to ground is proportional to the difference between the voltages at its two high impedance inputs.
interchannel delay	Amount of time that passes between sampling consecutive channels. The interchannel delay must be short enough to allow sampling of all the channels in the channel list, within the scan interval. The greater the interchannel delay, the more time the PGA is allowed to settle before the next channel is sampled. The interchannel delay is regulated by AI CONV CLK.

K

k	Kilo—The standard metric prefix for 1,000, or 10^3, used with units of measure such as volts, hertz, and meters.
kS	1,000 samples.

L

LabVIEW	Laboratory Virtual Instrument Engineering Workbench—A program development application based on the programming language G and used commonly for test and measurement purposes.
LED	Light-emitting diode.
linearity	The adherence of device response to the equation R = KS, where R = response, S = stimulus, and K = a constant.
LSB	Least significant bit.

M

MAX	Measurement & Automation Explorer—NI software for configuring devices and channels.
maximum working voltage	The highest voltage with respect to ground that should be applied to an input terminal during normal use, normally well under the breakdown voltage for safety margin. Includes both the signal and common-mode voltages.
MITE	MXI Interface to Everything—A custom ASIC designed by NI that implements the PCI bus interface. The MITE supports bus mastering for high-speed data transfers over the PCI bus.
MSB	Most significant bit.
mux	Multiplexer—A switching device with multiple inputs that sequentially connects each of its inputs to its output, typically at high speeds, in order to measure several signals with a single analog input channel.

N

NI-DAQmx	The latest NI-DAQ driver with new VIs, functions, and development tools for controlling measurement devices.
noise	An undesirable electrical signal—Noise comes from external sources such as the AC power line, motors, generators, transformers, fluorescent lights, soldering irons, CRT displays, computers, electrical storms, welders, radio transmitters, and internal sources such as semiconductors, resistors, and capacitors. Noise corrupts signals you are trying to send or receive.

normal mode voltage	Voltage that occurs in the case of interference between two conductors of a circuit.

O

OUT	Output pin—A counter output pin where the counter can generate various TTL pulse waveforms.

P

PCI	Peripheral component interconnect.
PFI	Programmable function input.
PGA	Programmable gain amplifier.
port	(1) A communications connection on a computer or a remote controller; (2) a digital port, consisting of four or eight lines of digital input and/or output.
ppm	Parts per million.
PXI	PCI eXtensions for Instrumentation—An open specification that builds on the CompactPCI specification by adding instrumentation-specific features.
PXI trigger bus	The timing bus that connects PXI DAQ devices directly, by means of connectors built into the backplane of the PXI chassis, for precise synchronization of functions. This bus is functionally equivalent to the RTSI bus for PCI DAQ devices.

R

relative accuracy	A measure in LSB of the accuracy of an ADC. It includes all nonlinearity and quantization errors. It does not include offset and gain errors of the circuitry feeding the ADC.
resolution	The smallest signal increment that can be detected by a measurement system. Resolution can be expressed in bits, in proportions, or in percent of full scale. For example, a system has 16-bit resolution, one part in 65,536 resolution, and 0.0015% of full scale.

rms	Root mean square—The square root of the average value of the square of the instantaneous signal amplitude; a measure of signal amplitude.
RTSI bus	Real-time system integration bus—The NI timing bus that connects DAQ devices directly, for precise synchronization of functions.

S

s	Second or seconds.
S	Sample or samples.
S/s	Samples per second—Used to express the rate at which a DAQ device samples an analog signal.
sample counter	The clock that counts the output of the channel clock, in other words, the number of samples taken.
scan	One or more analog or digital input samples. Typically, the number of input samples in a scan is equal to the number of channels in the input group. For example, one pulse from the scan clock produces one scan which acquires one new sample from every analog input channel in the group.
scan clock	The clock controlling the time interval between scans.
scan interval	Controls how often a scan is initialized. The scan interval is regulated by AI SAMP CLK.
scan rate	Reciprocal of the scan interval.
SCXI	Signal Conditioning eXtensions for Instrumentation—The NI product line for conditioning low-level signals within an external chassis near sensors so only high-level signals are sent to DAQ devices in the noisy PC environment.
self-calibrating	A property of a DAQ device that has an extremely stable onboard reference and calibrates its own A/D and D/A circuits without manual adjustments by the user.
signal conditioning	The manipulation of signals to prepare them for digitizing.
software trigger	A programmed event that triggers an event such as DAQ.
STC	System timing controller.

T

TRIG	Trigger signal.
trigger	Any event that causes or starts some form of data capture.
TTL	Transistor-transistor logic—A digital circuit composed of bipolar transistors wired in a certain manner.

V

V	Volt or volts.
VDC	Volts direct current.
VI	Virtual instrument—(1) A combination of hardware and/or software elements, typically used with a PC, that has the functionality of a classic stand-alone instrument; (2) a LabVIEW software device (VI), which consists of a front panel user interface and a block diagram program.
V_{MEAS}	Measured voltage.
V_{rms}	Volts, root mean square.

W

waveform	Multiple voltage readings taken at a specific sampling rate.
working voltage	The highest voltage with respect to ground that should be applied to an input terminal during normal use, normally well under the breakdown voltage for safety margin. Includes both the signal and common-mode voltages.

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